
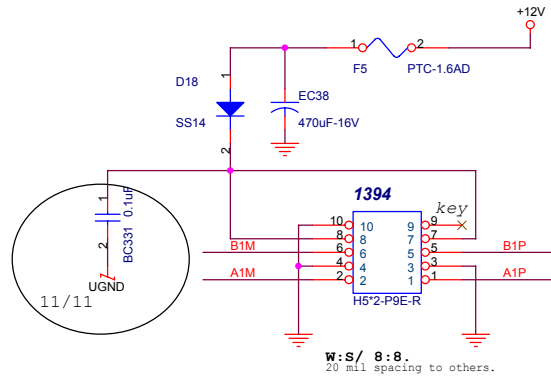
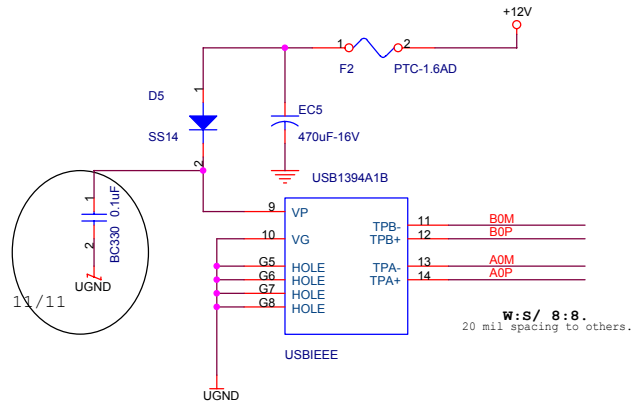
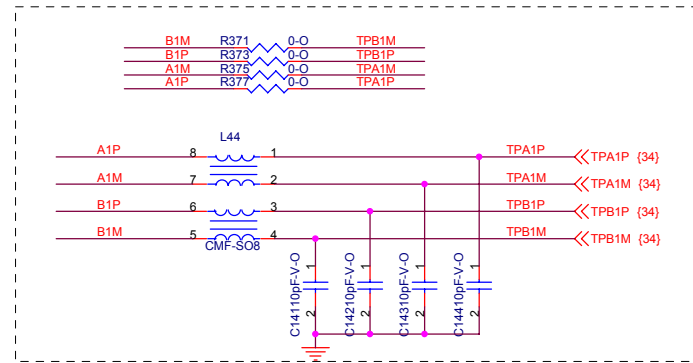
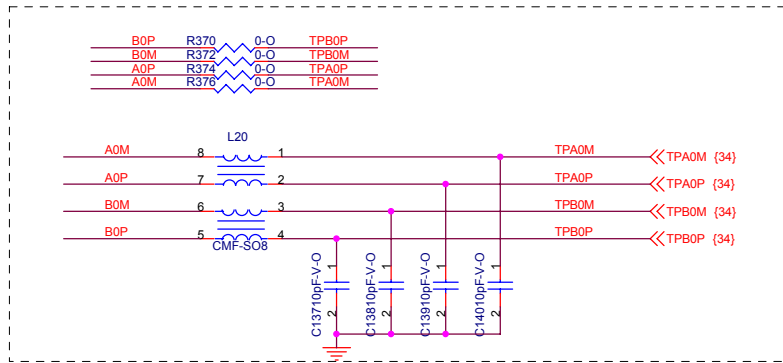


1	2	3	4	5	6	7	8
A							A
B							B
C							C
D							D



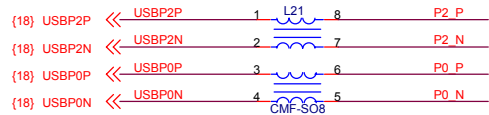
Elitegroup Computer Systems

Title		
Schematic Change History		
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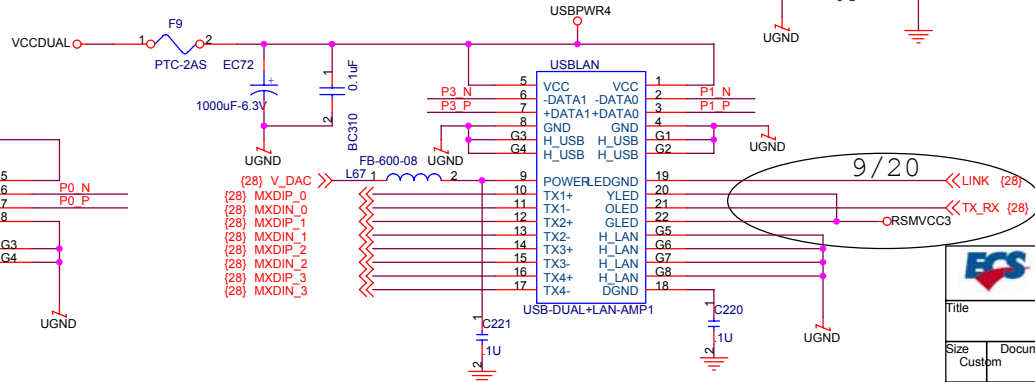
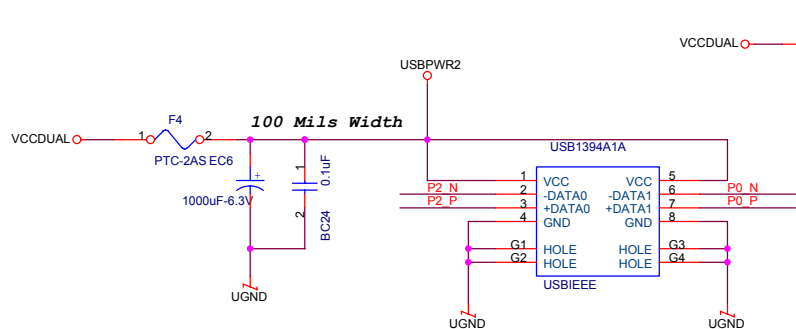
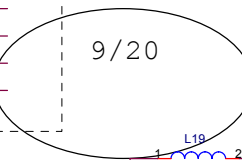
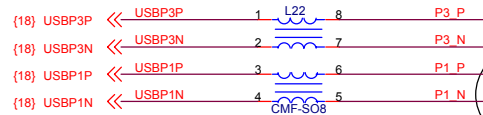
REAR_SIDE

USBP0N	R378	0-0	P0_N
USBP0P	R380	0-0	P0_P
USBP2N	R382	0-0	P2_N
USBP2P	R384	0-0	P2_P



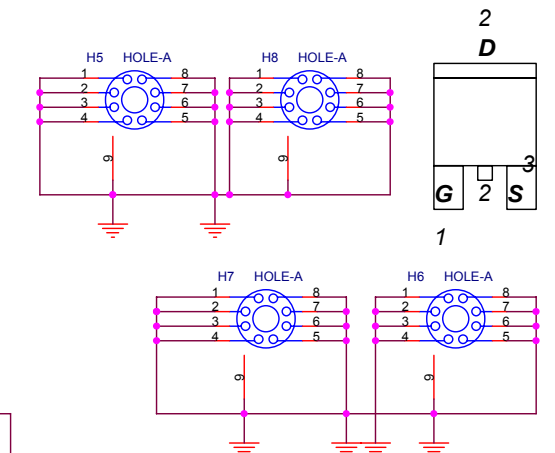
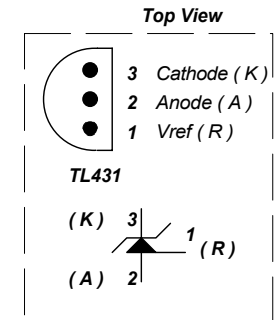
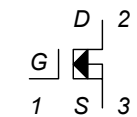
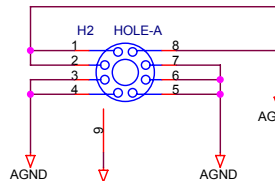
REAR_SIDE

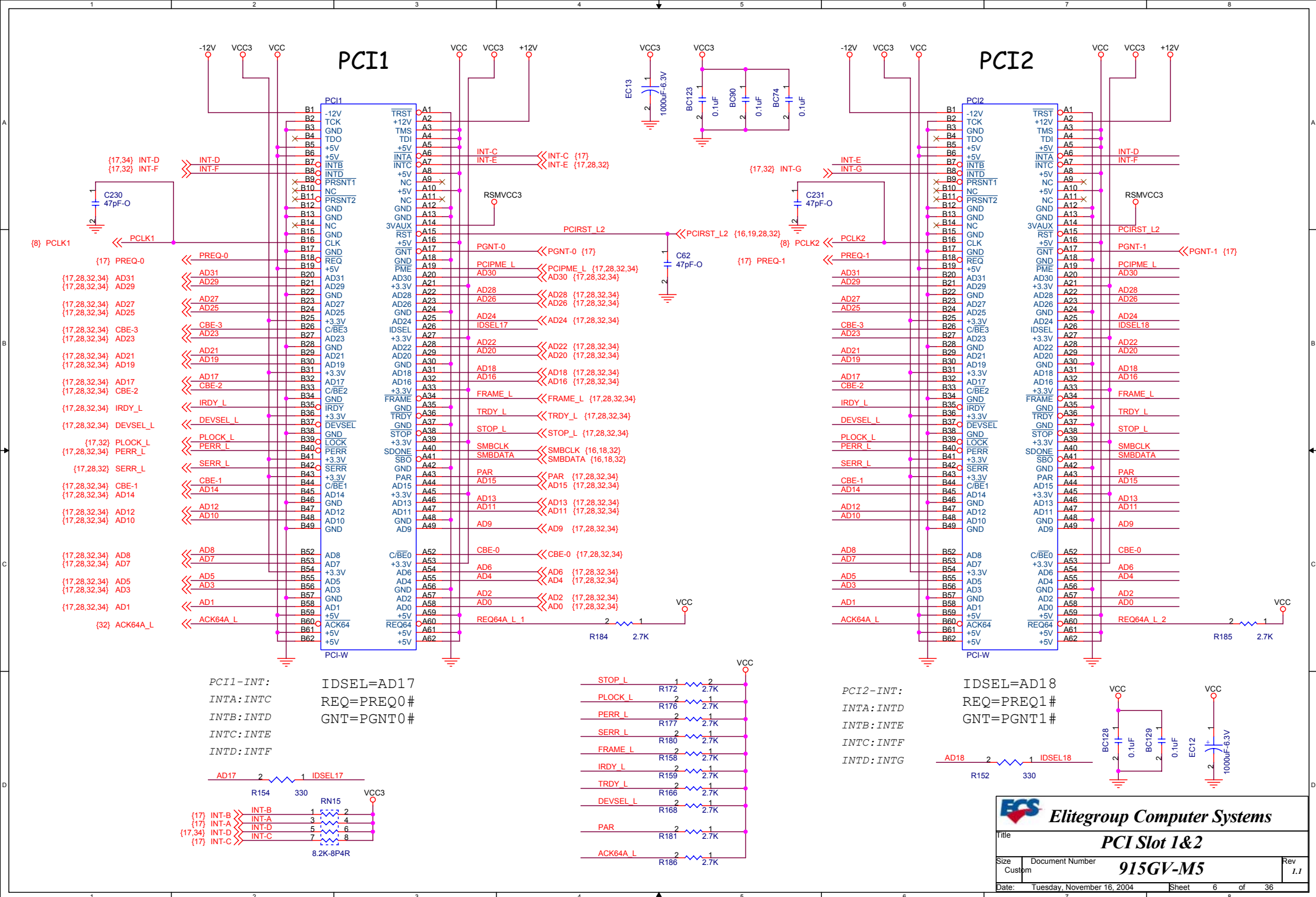
USBP1N	R379	0-0	P1_N
USBP1P	R381	0-0	P1_P
USBP3N	R383	0-0	P3_N
USBP3P	R385	0-0	P3_P

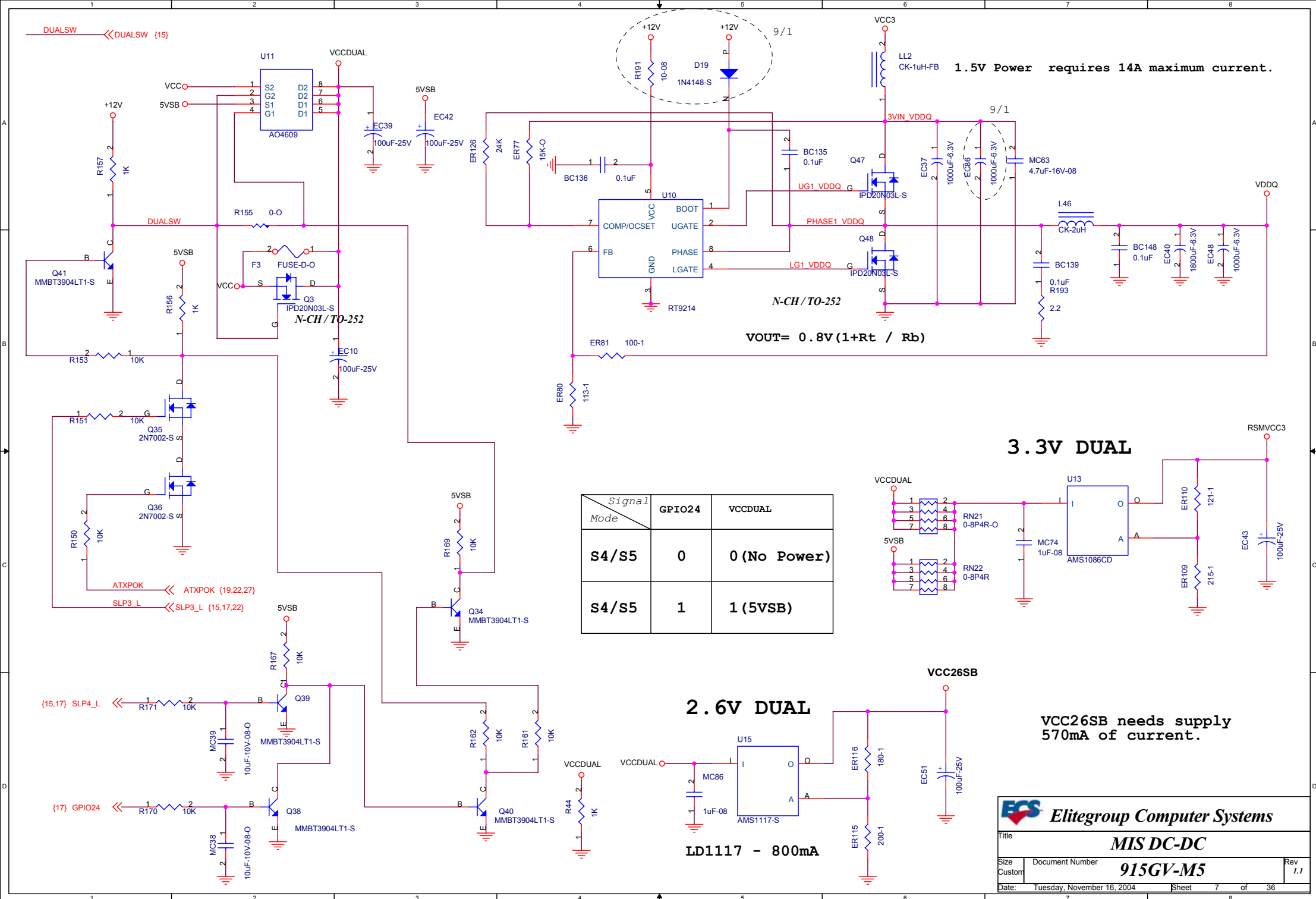


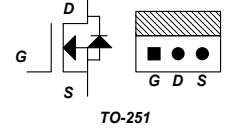
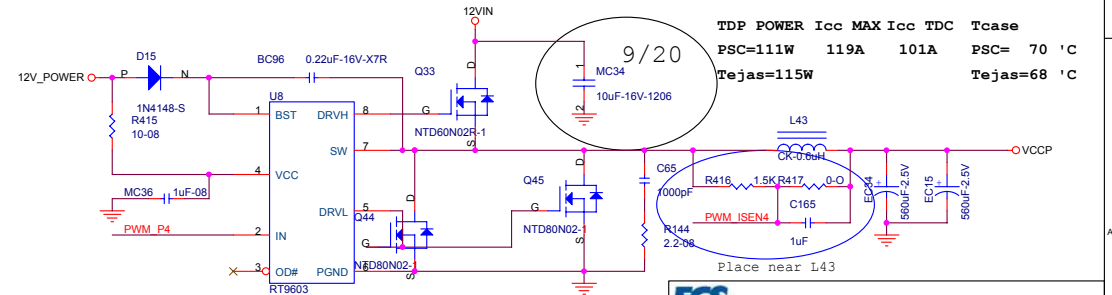
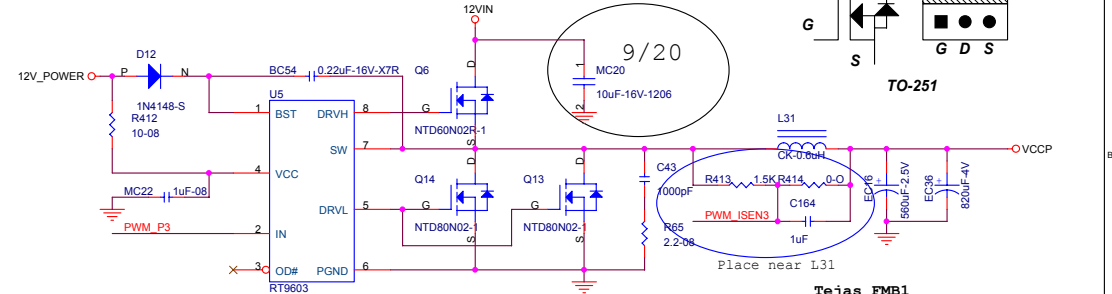
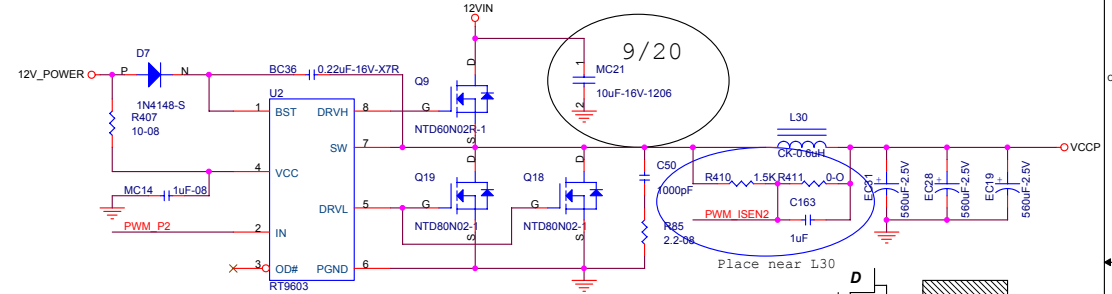
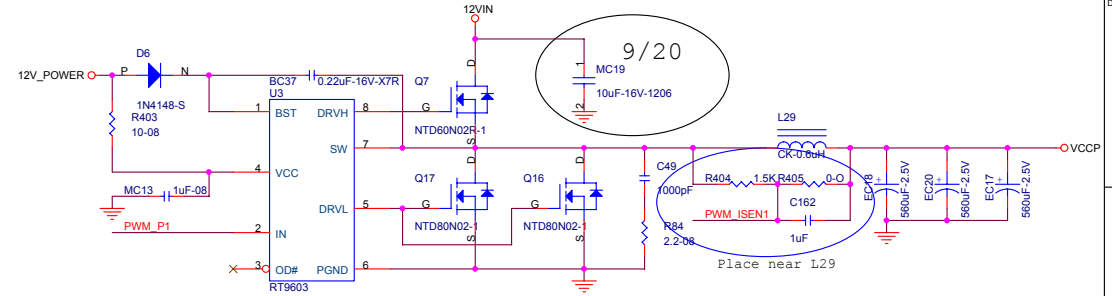
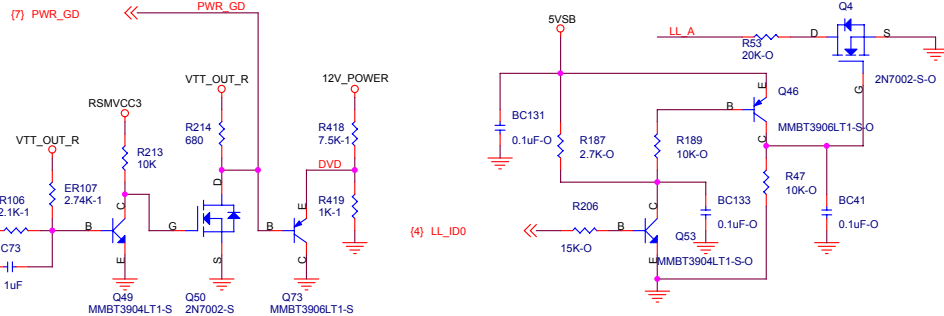
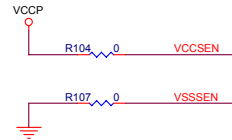
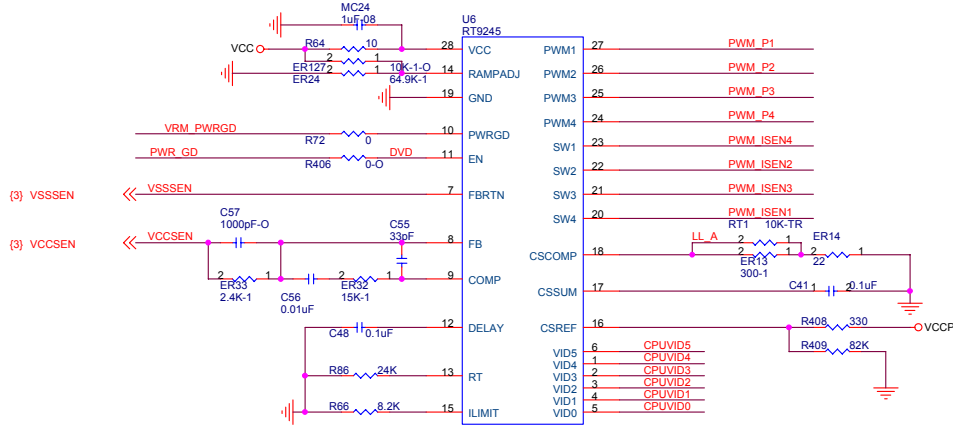
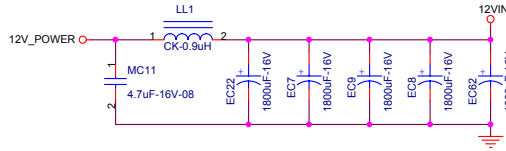
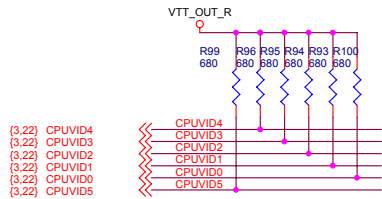
Elitegroup Computer Systems

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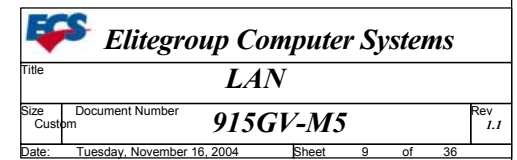


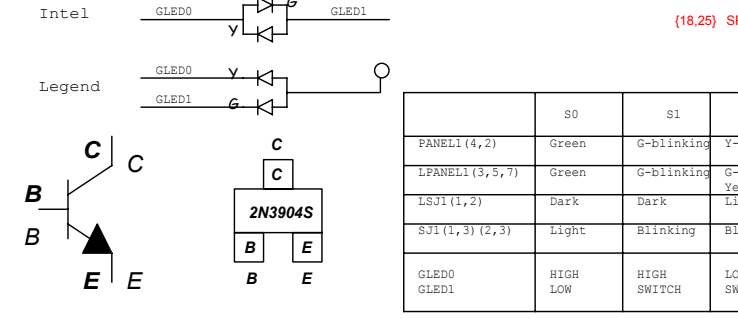
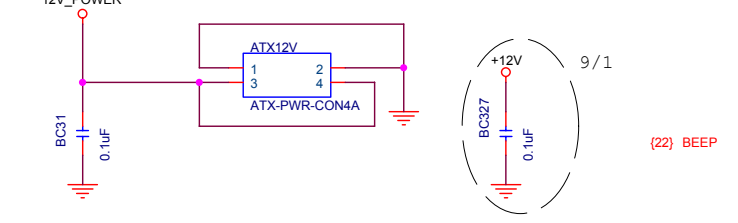
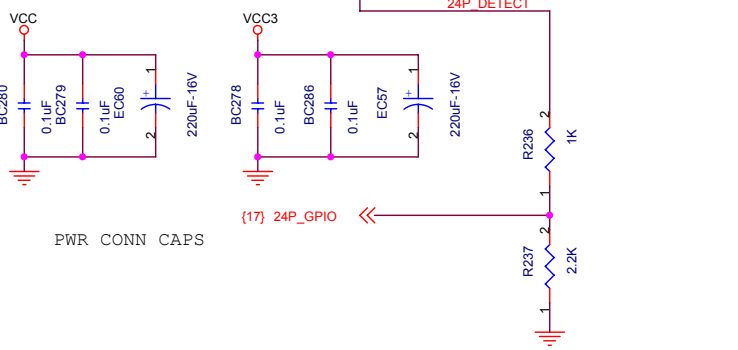
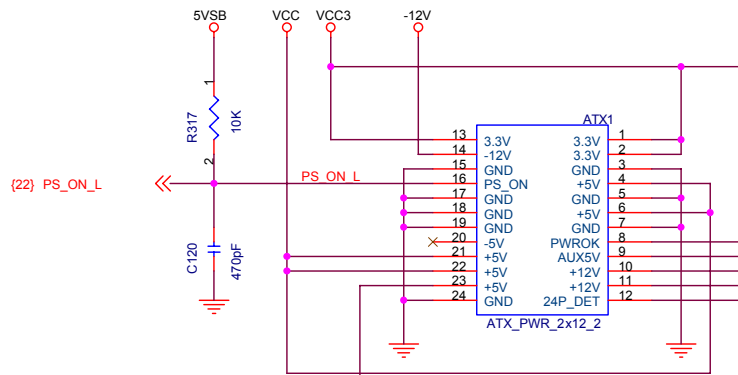




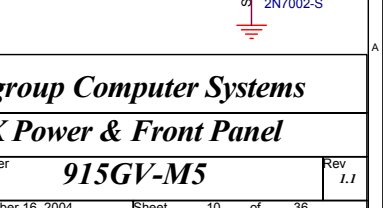
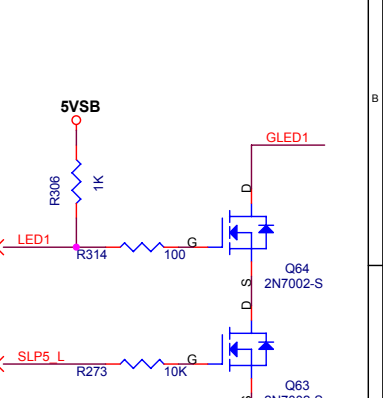
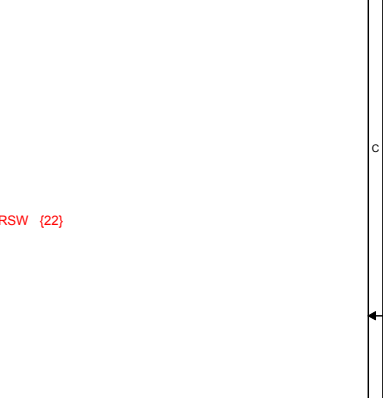
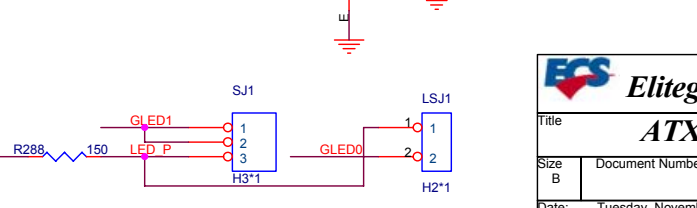
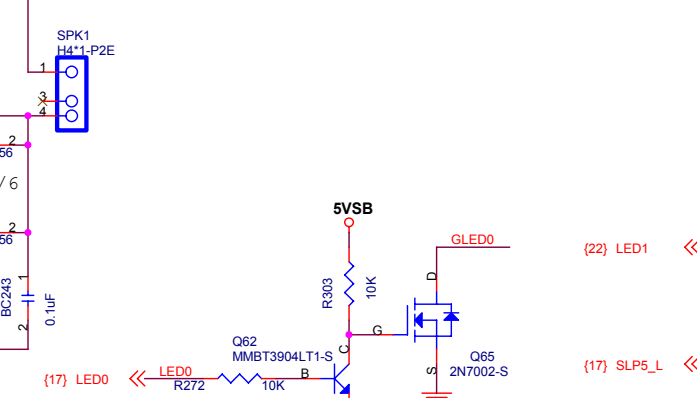
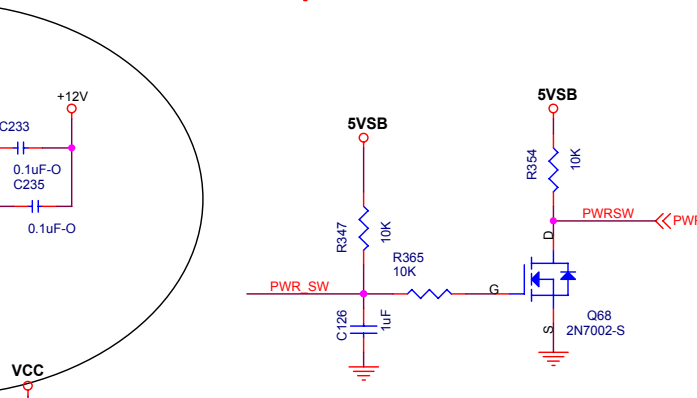
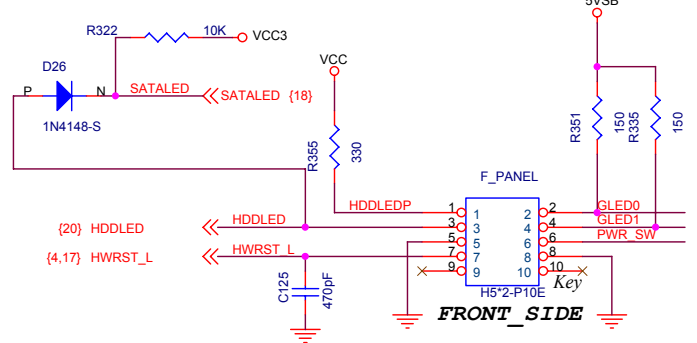
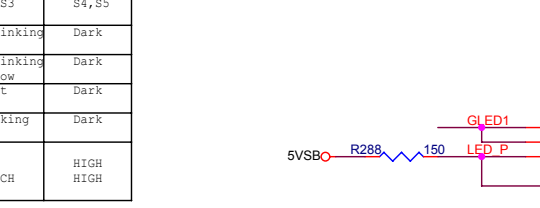
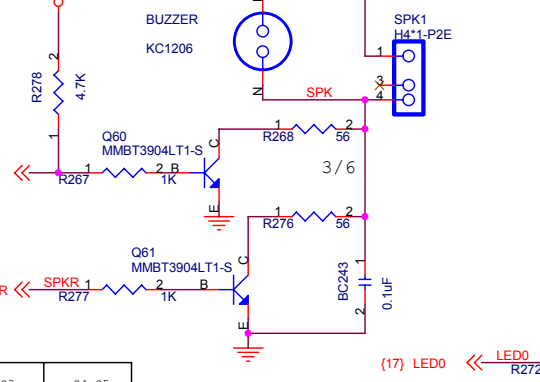
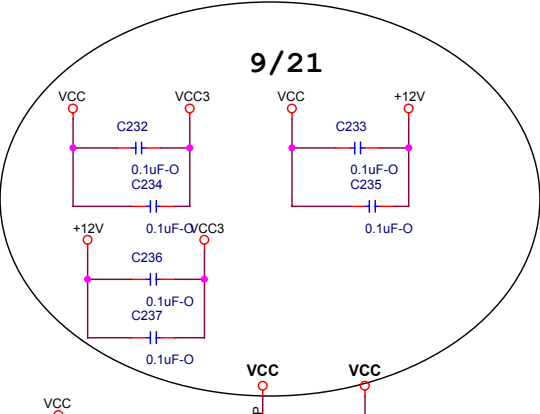
Tejas FMB1

TDP POWER	Icc MAX	Icc TDC	Tc case
PSC=111W	119A	101A	PSC= 70 'C
Tejas=115W			Tejas=68 'C





	S0	S1	S3	S4,S5
PANEL1 (4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1 (3,S,7)	Green	G-blinking	G-blinking	Dark
LSJ1 (1,2)	Dark	Dark	Light	Dark
SJ1 (1,3) (2,3)	Light	Blinking	Blinking	Dark
GLED0	HIGH	HIGH	LOW	HIGH
GLED1	LOW	SWITCH	SWITCH	HIGH



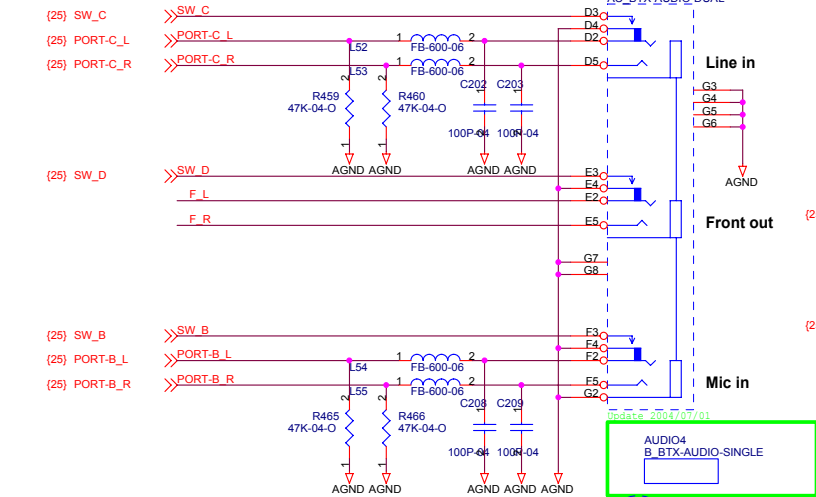
Elitegroup Computer Systems

Title: **ATX Power & Front Panel**

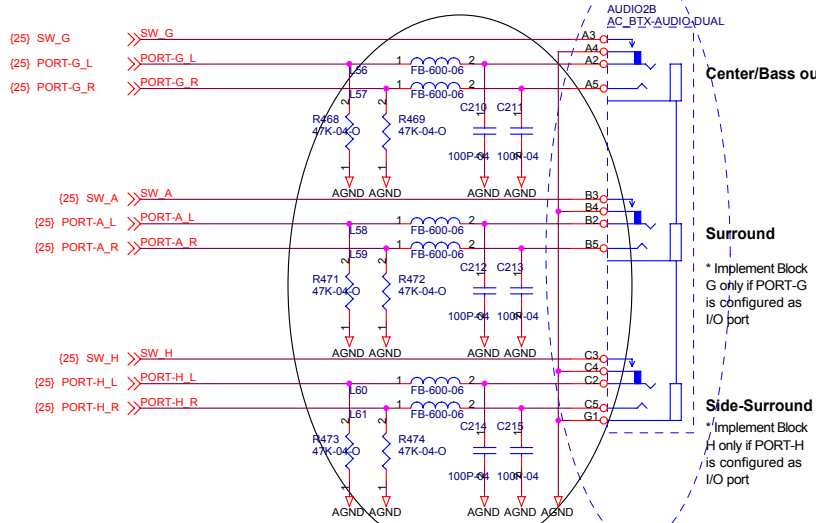
Size B Document Number: **915GV-M5** Rev 1.1

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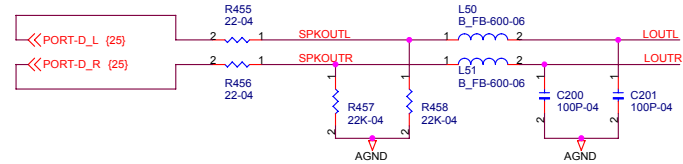
Rear Panel Onboard Analog I/O



Rear Panel (Optional Rear Audio Panel)



The schematic should consist with PINs define of I/O connector.

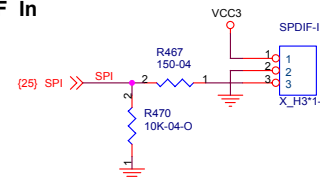


(25) F_MIC1

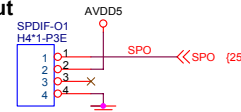
(25) F_MIC2

SPDIF I/O

SPDIF In



SPDIF Out



9/21

ALC880

ALC655

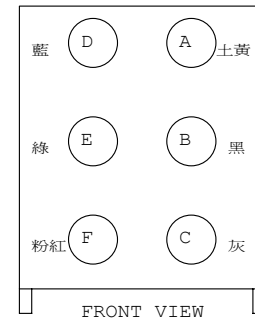
A

B

Line in

Front out

Mic in

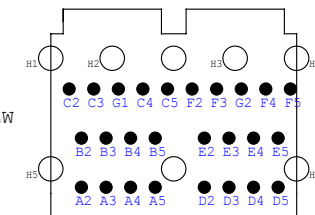


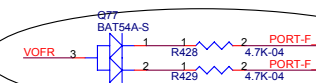
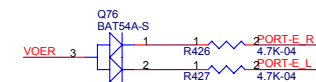
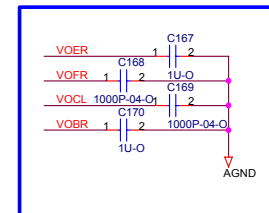
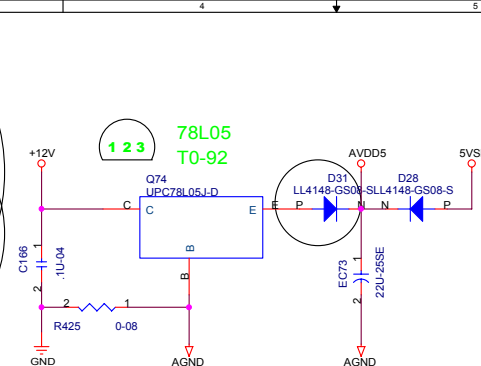
Center/Bass out

Back-Surround

Side-Surround

TOP VIEW





NetA

AVDD5

R430 1K-1-04-O

R431 5.1K-1-04

R433 10K-1-04

R434 20K-1-04

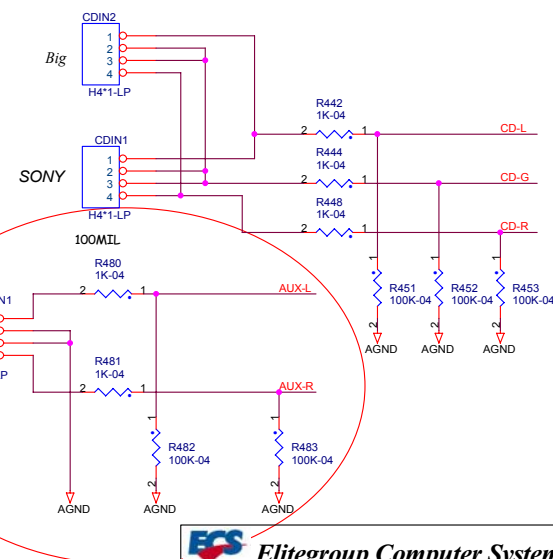
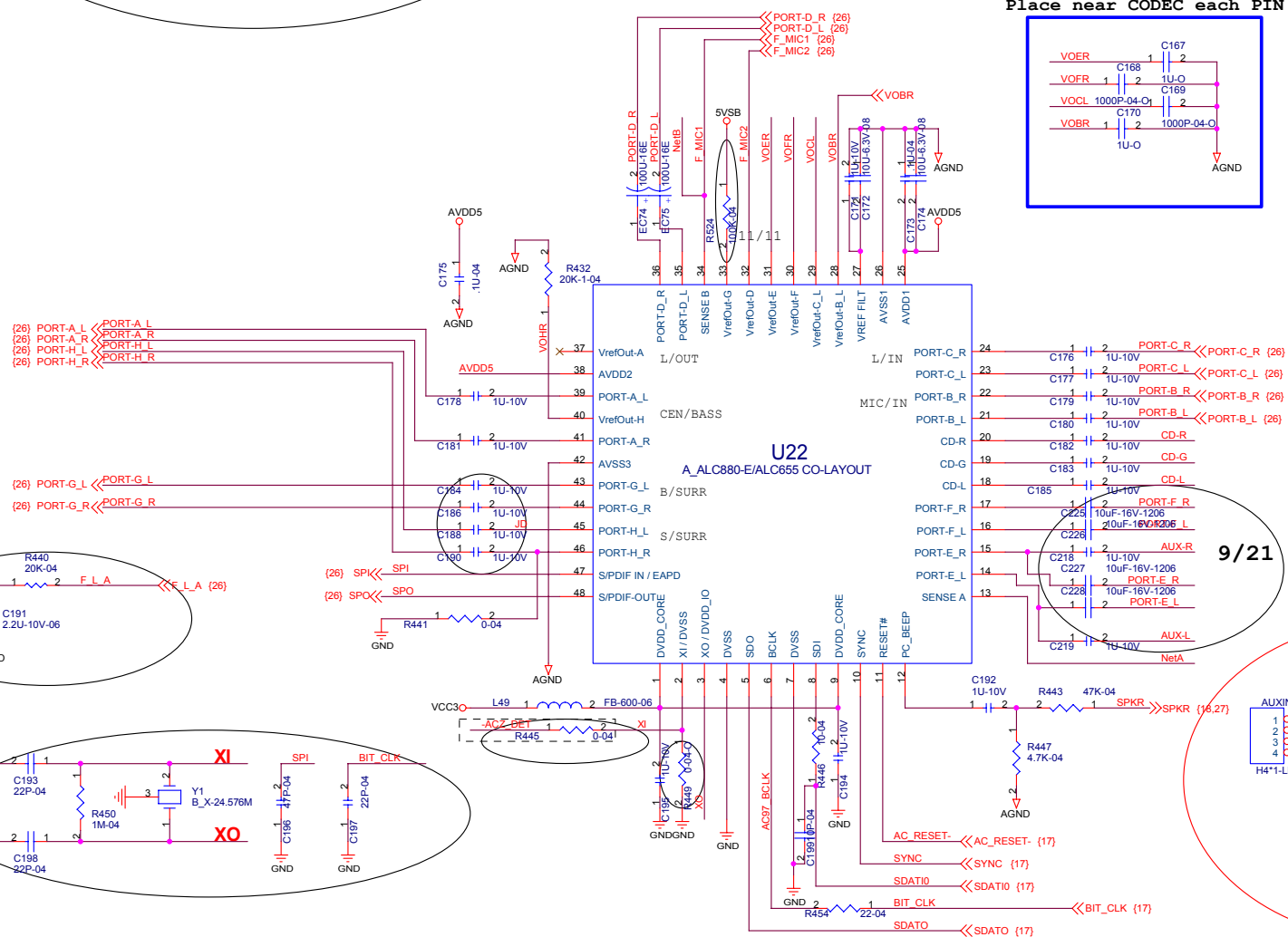
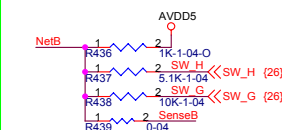
R435 39.2K-1-04

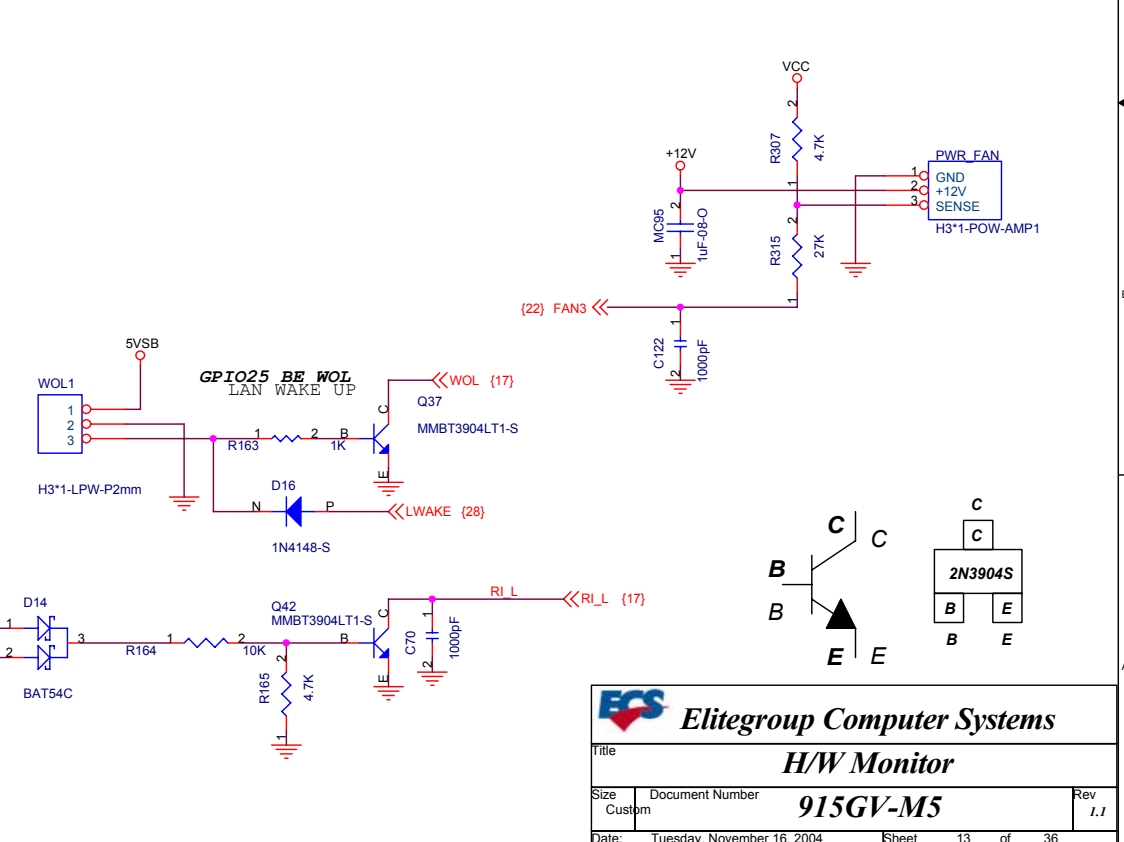
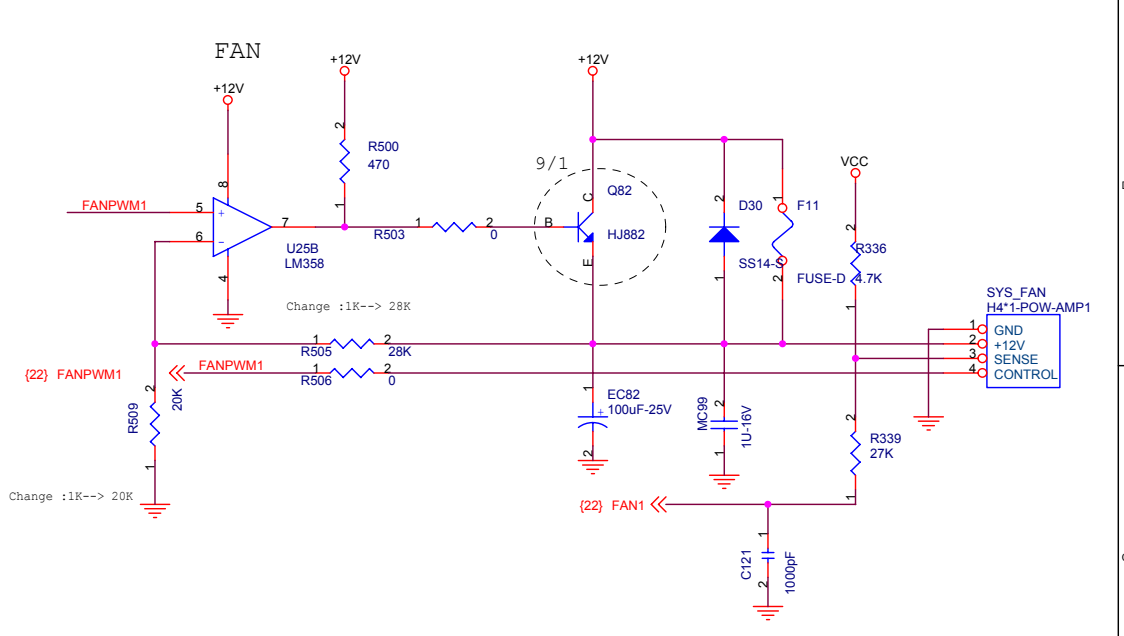
SW_D (26)

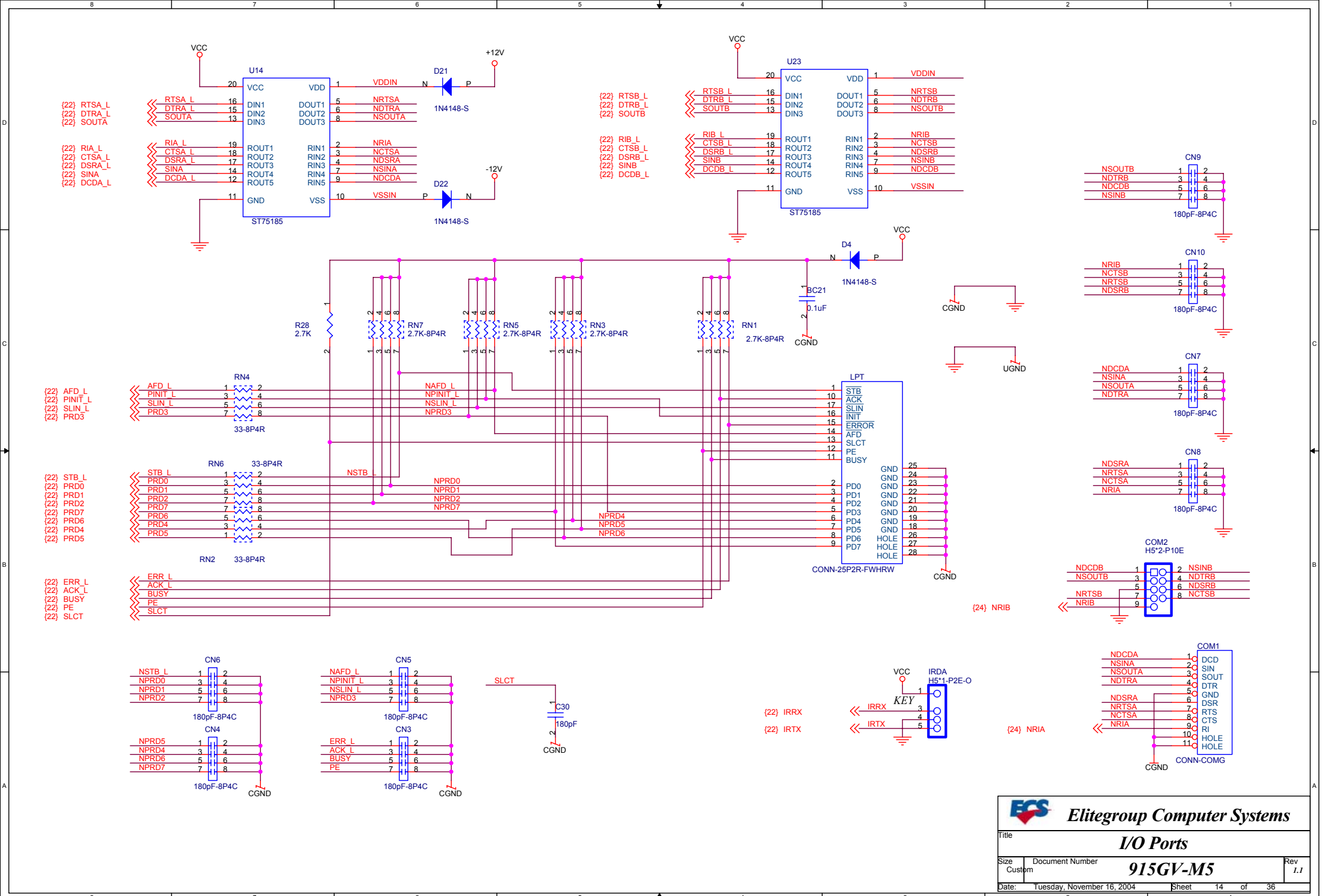
SW_C (26)

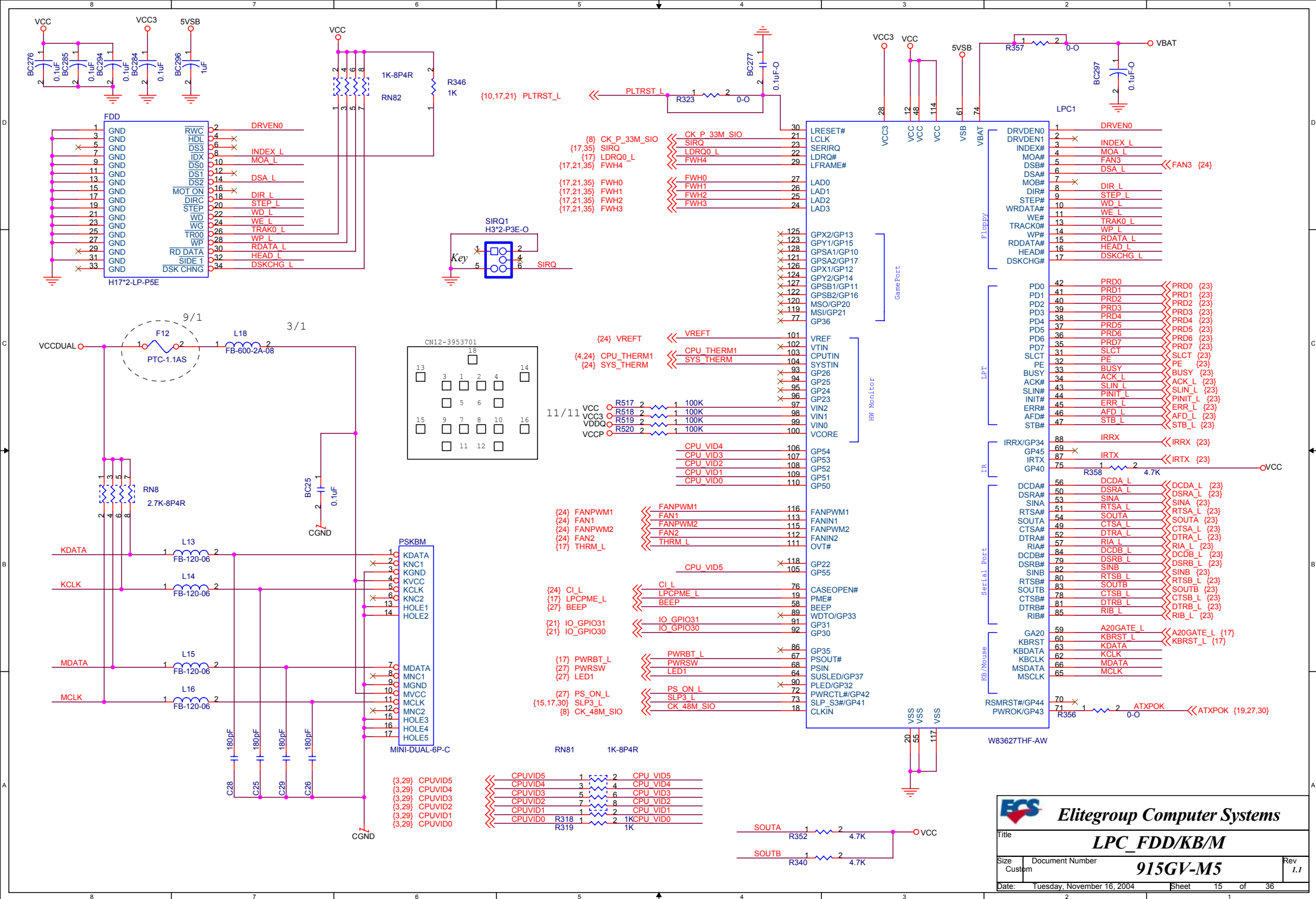
SW_B (26)

SW_A (26)

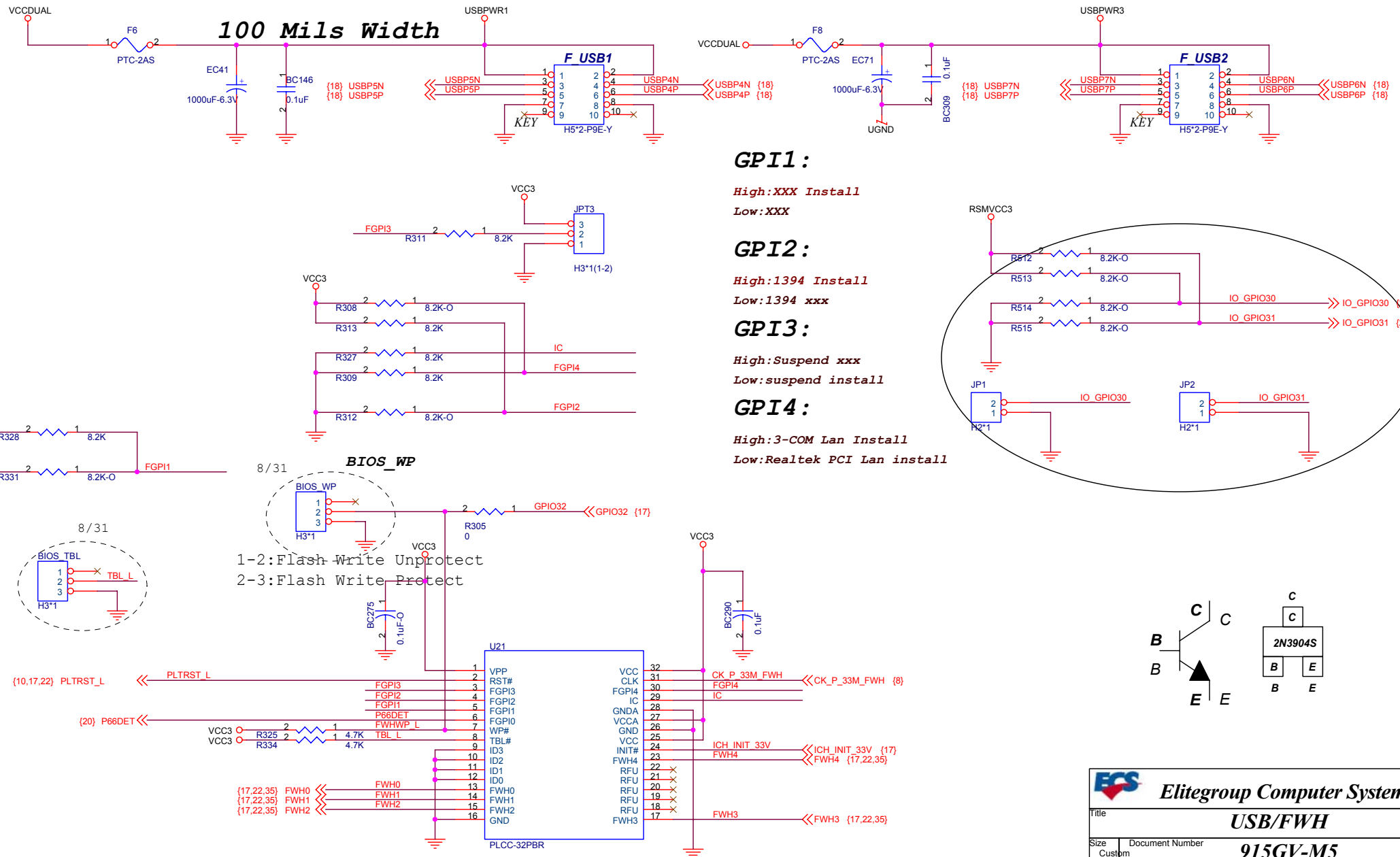








USB PORT INTERFACE



GPI1:

High:XXX Install

Low:XXX

GPI2:

High:1394 Install

Low:1394 xxx

GPI3:

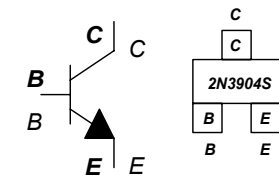
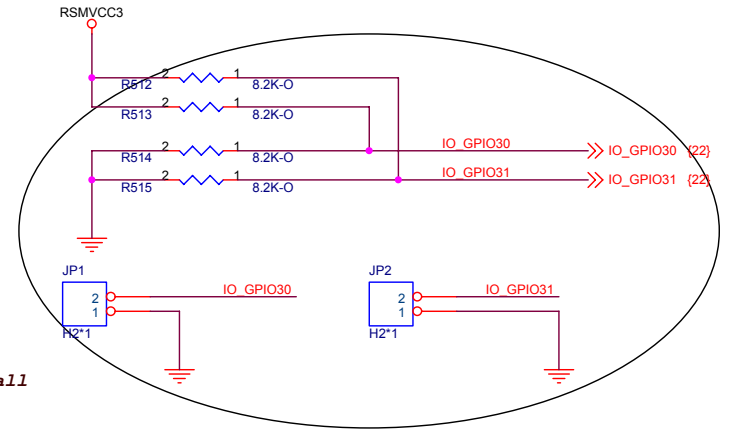
High:Suspend xxx

Low:suspend install

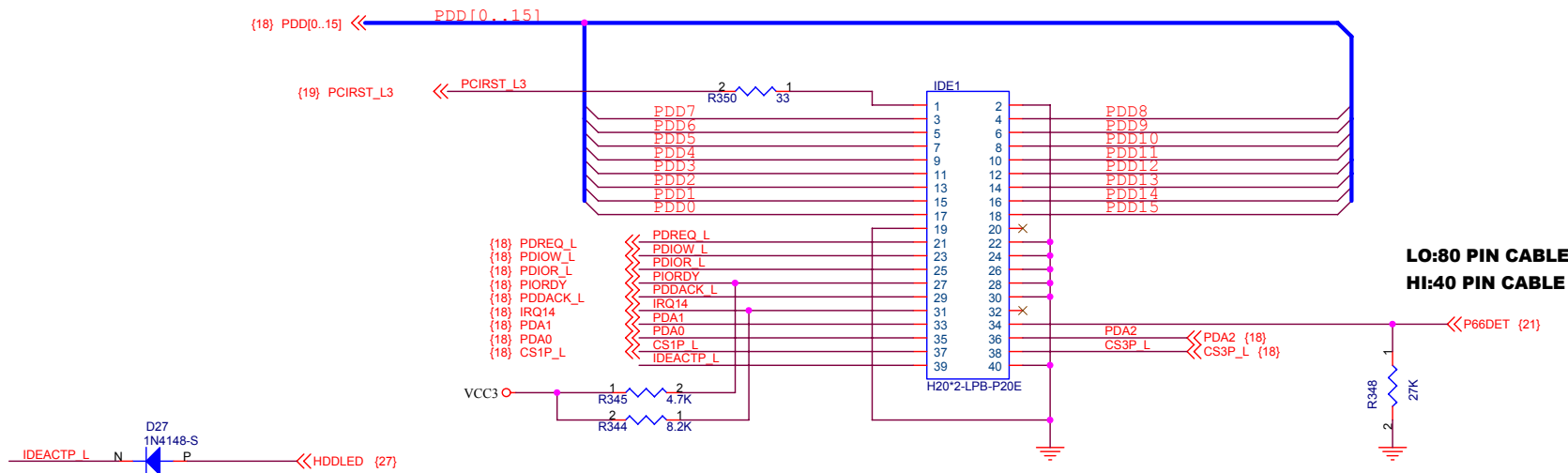
GPI4:

High:3-COM Lan Install

Low:Realtek PCI Lan install

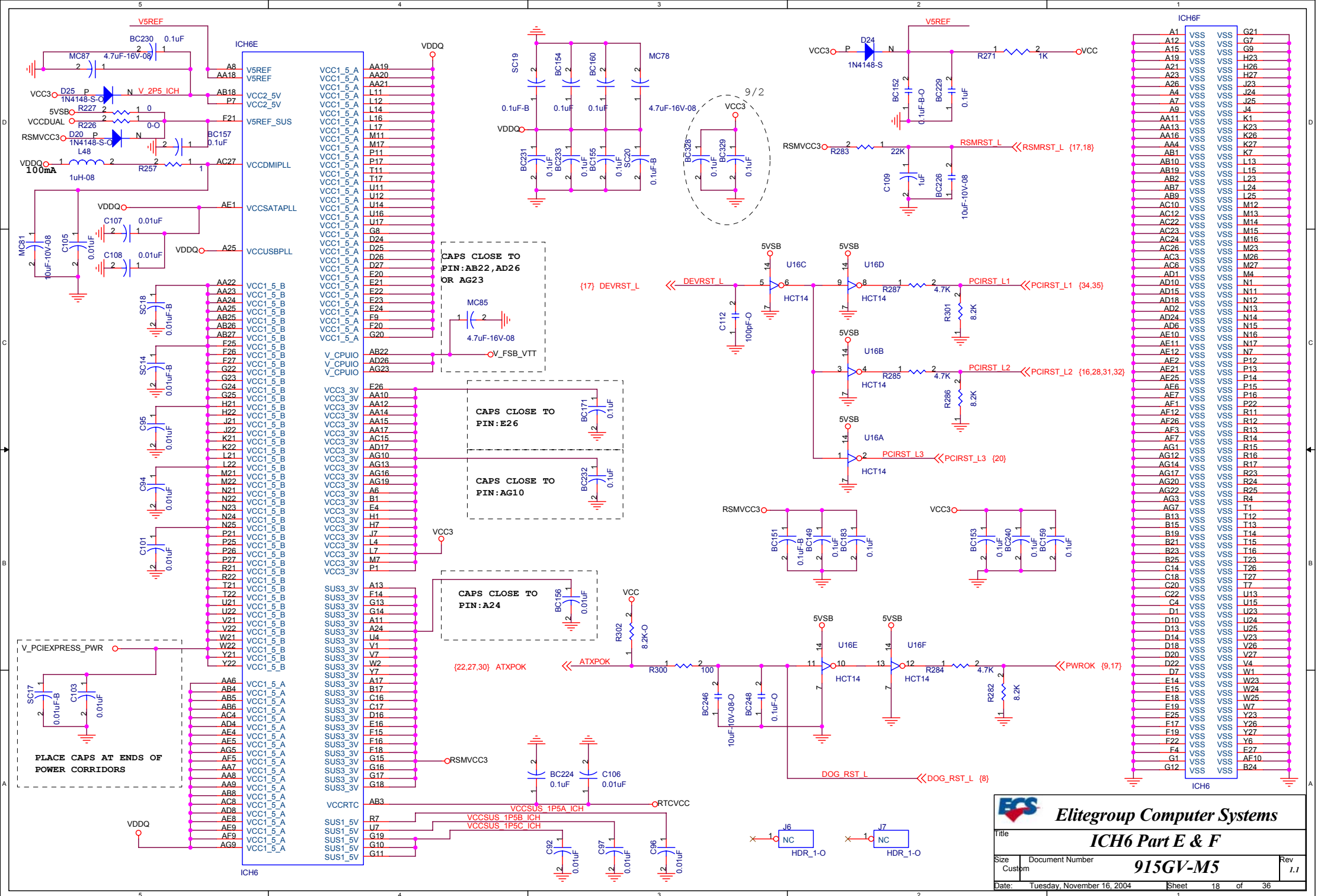


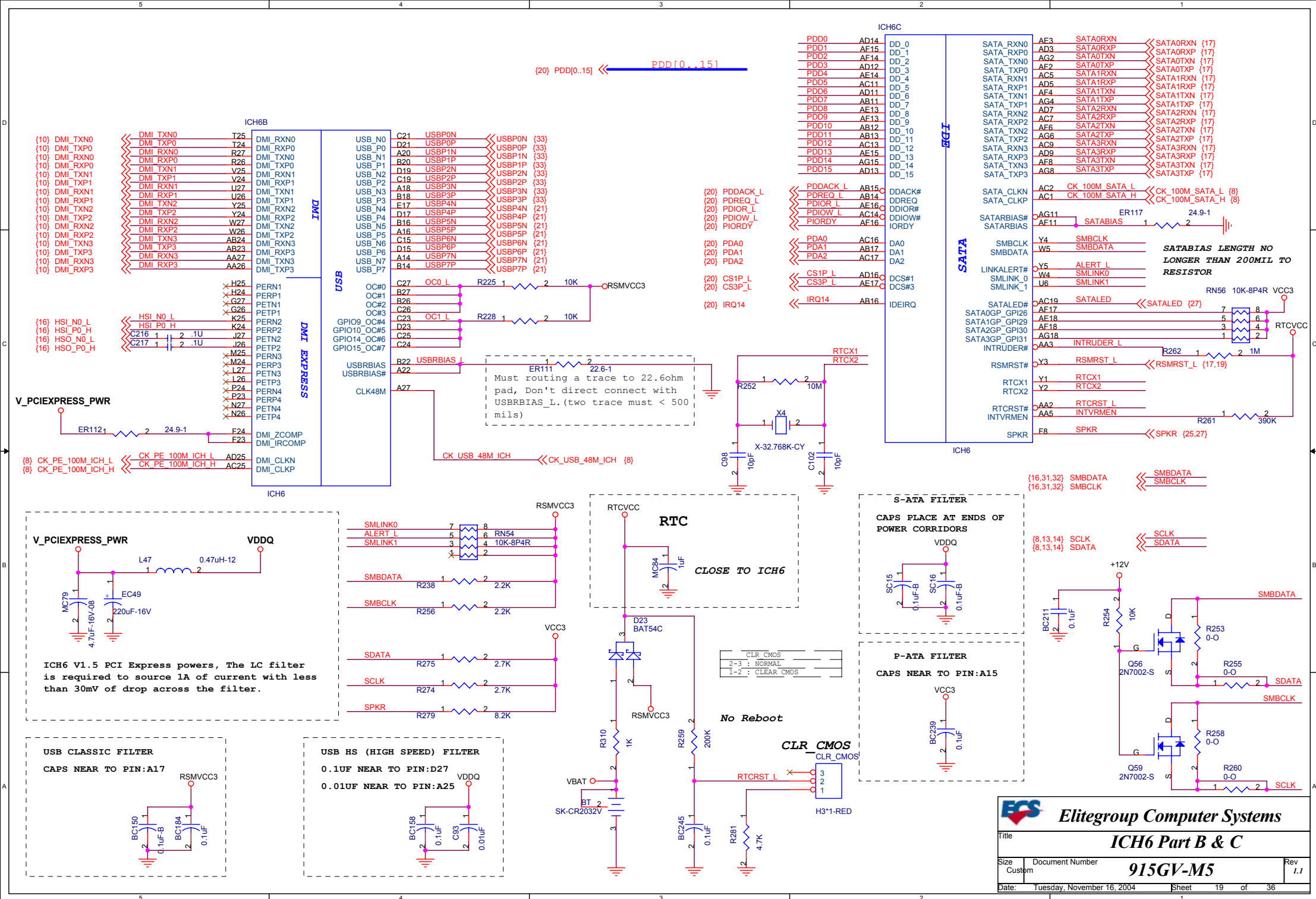
Title		
USB/FWH		
Size	Document Number	Rev
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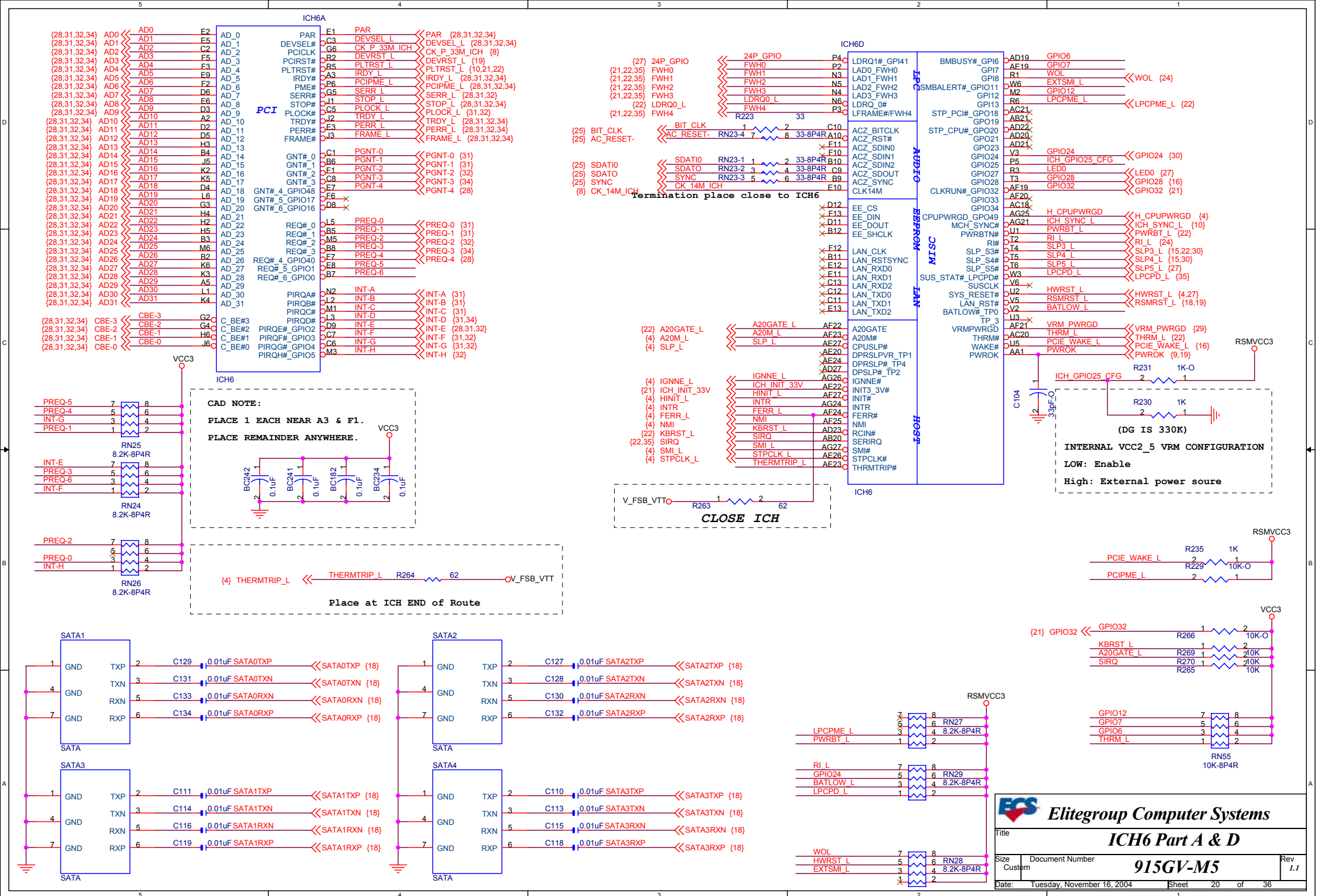


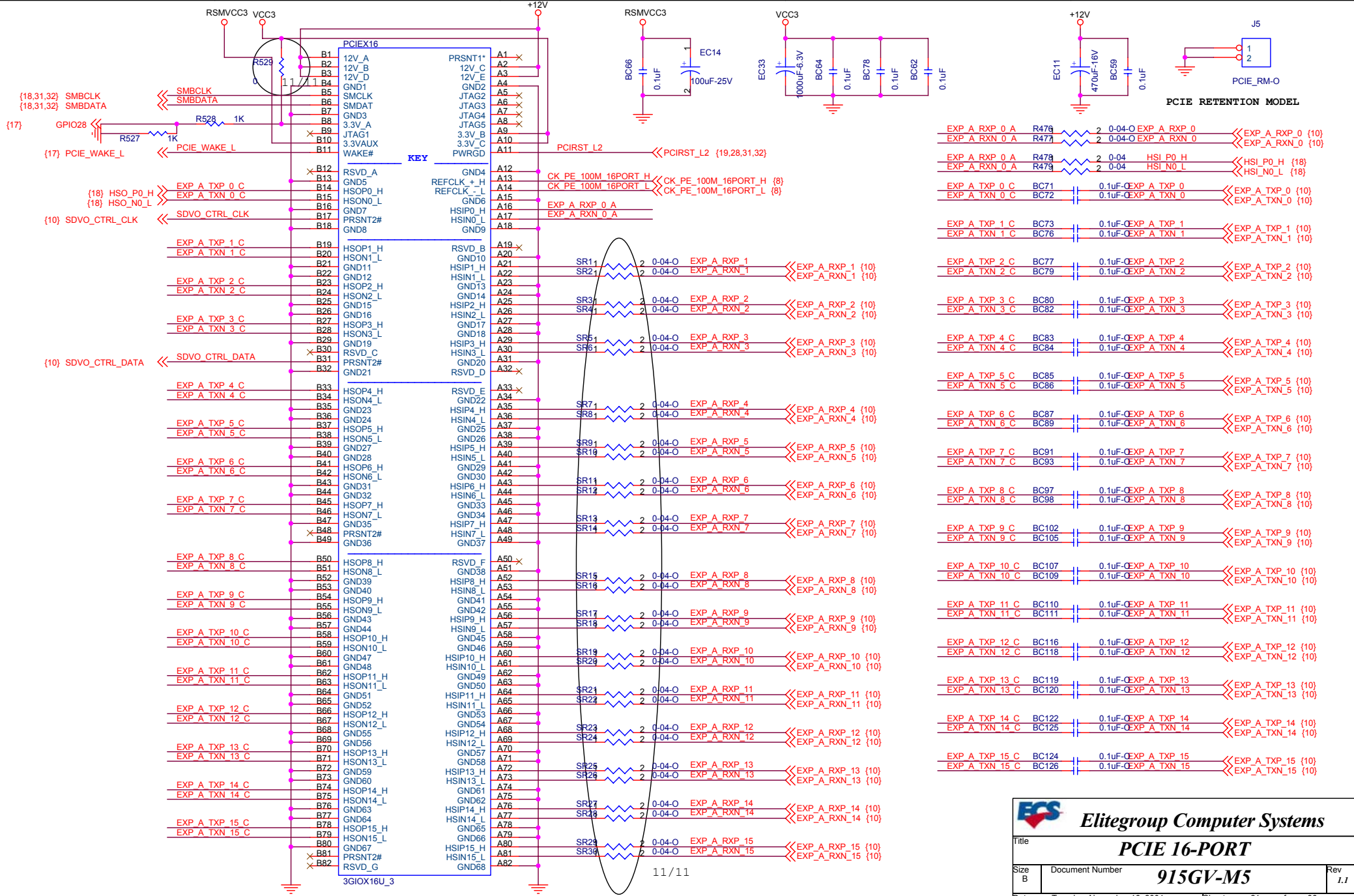
MAX TRACE LENGTH IS 8"

DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR_L , XIORDY_L) WITHIN +/- 250 MIL,
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.



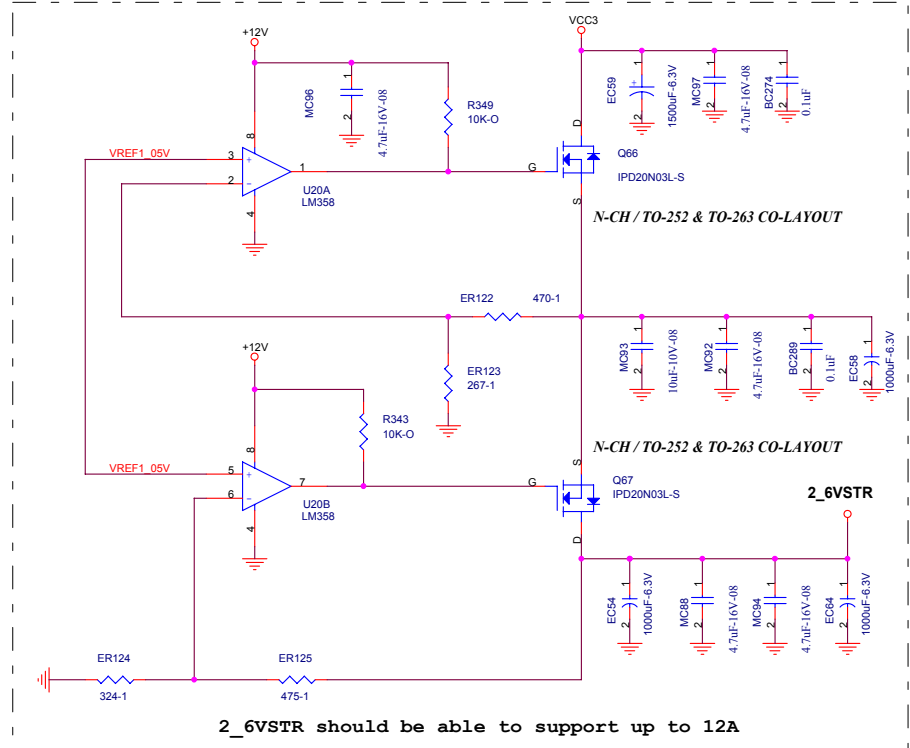
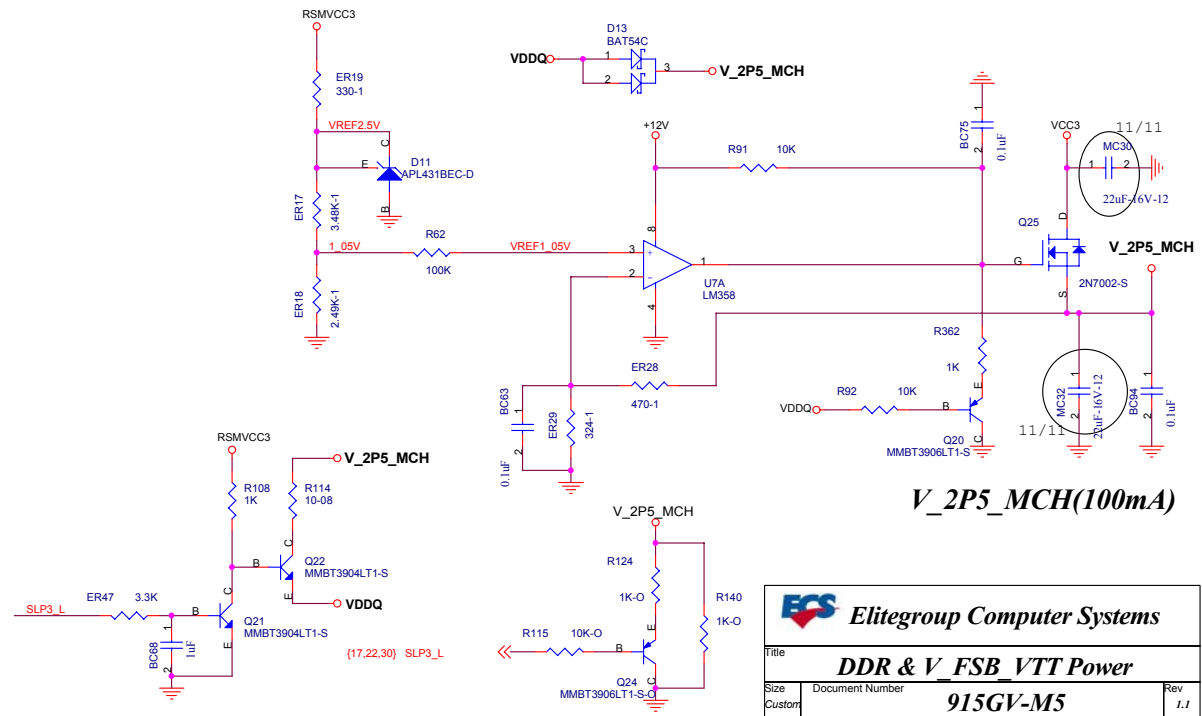
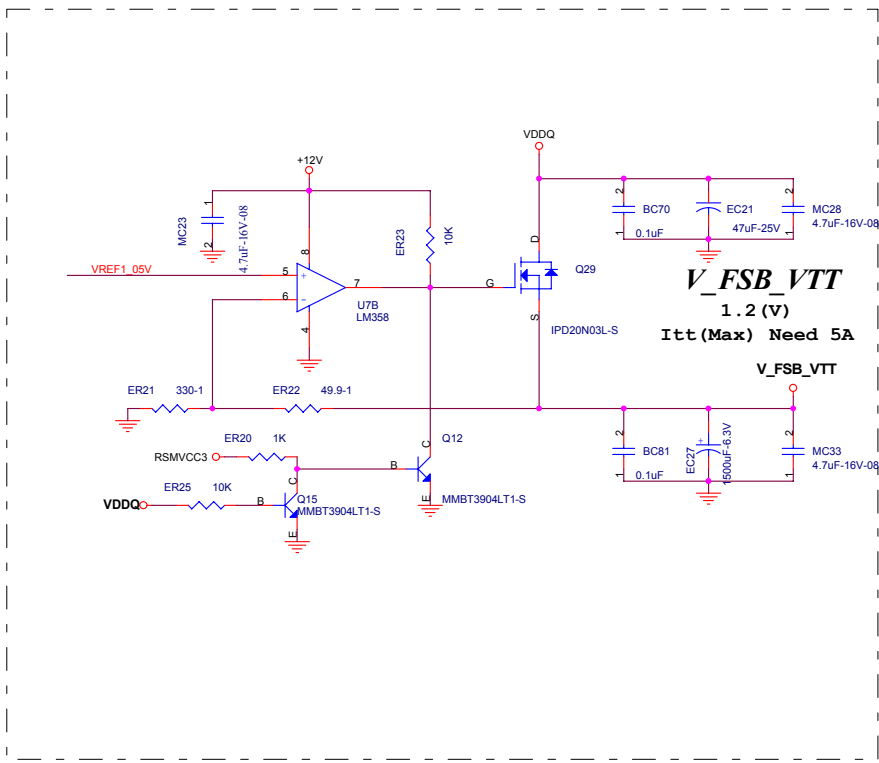
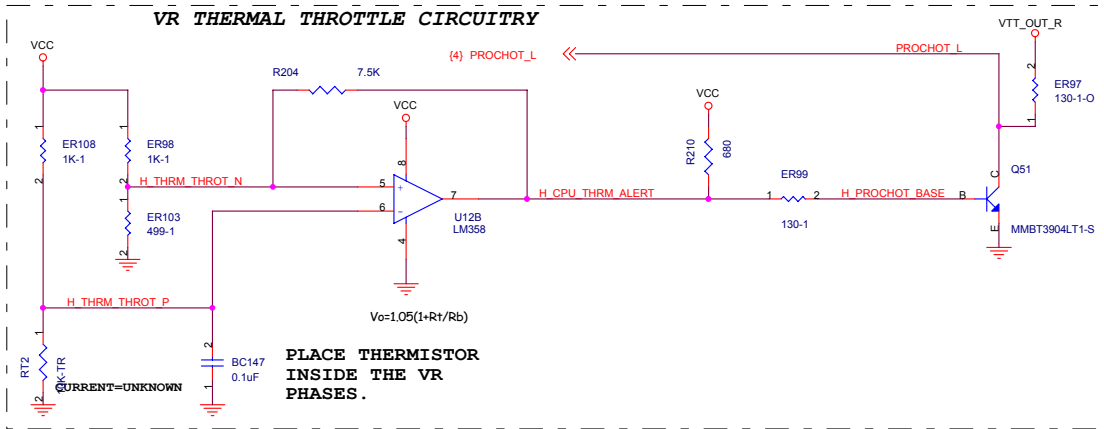
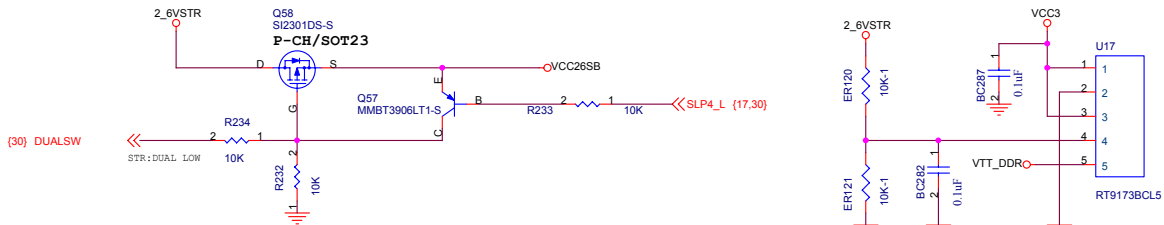


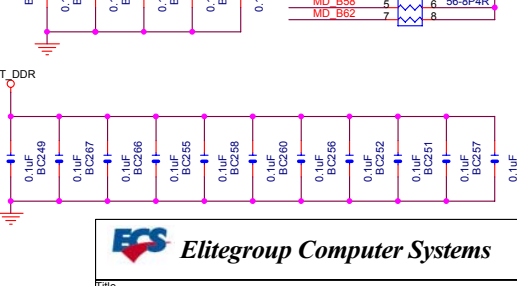
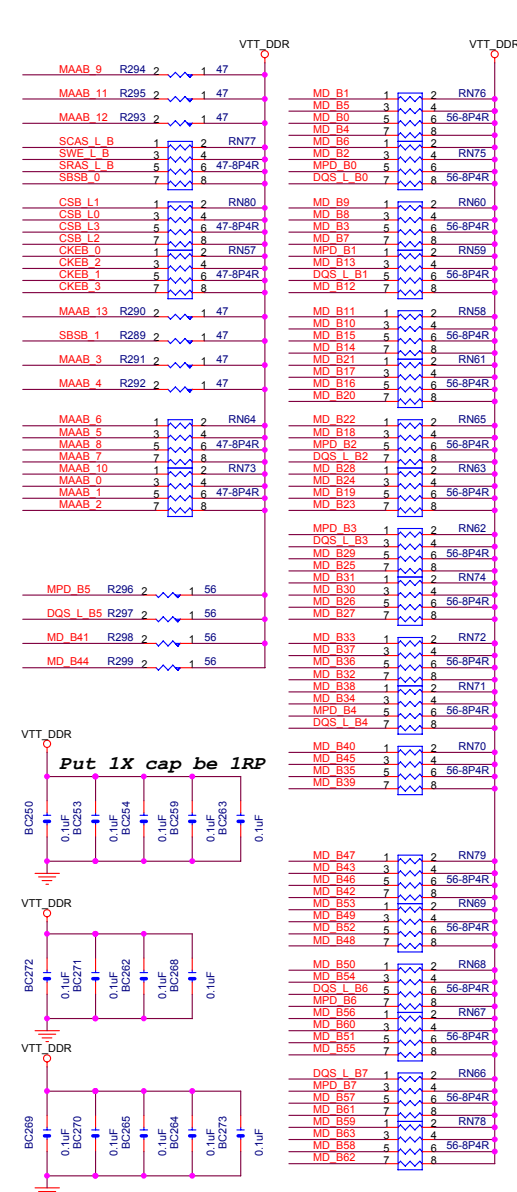
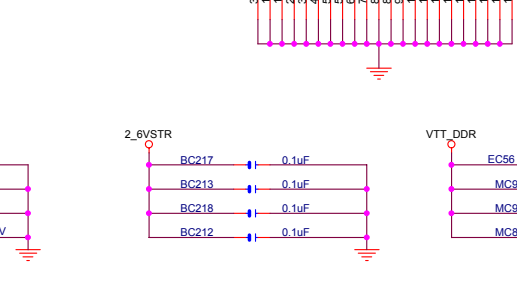
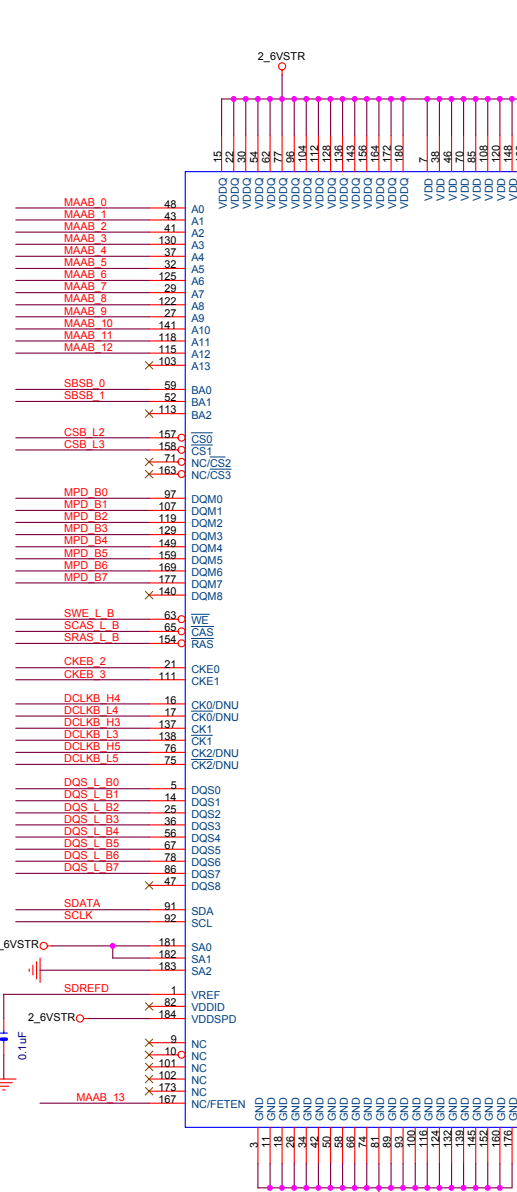
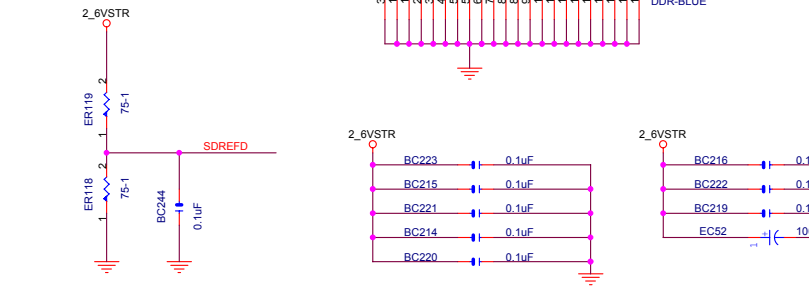
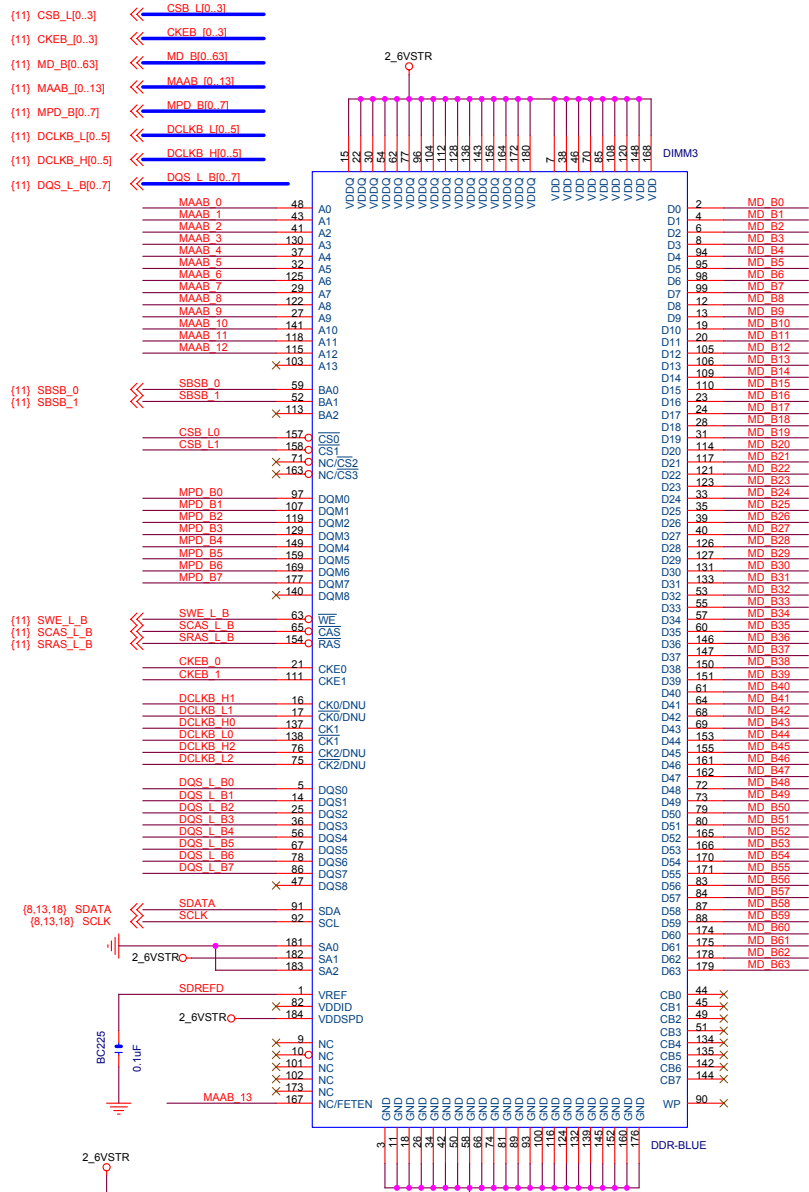


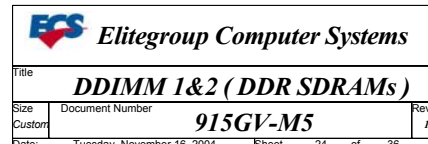


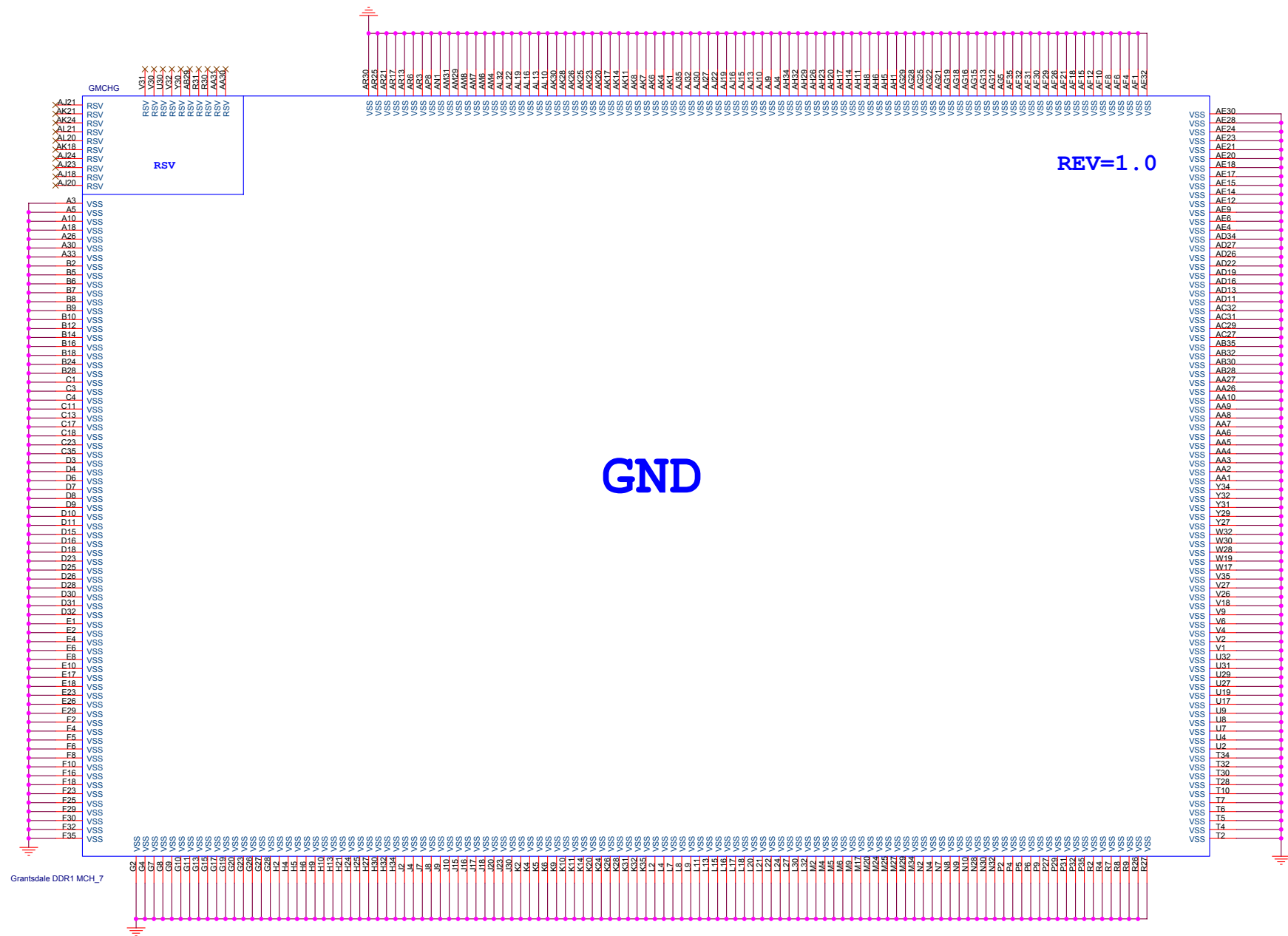
PCIE 16-PORT

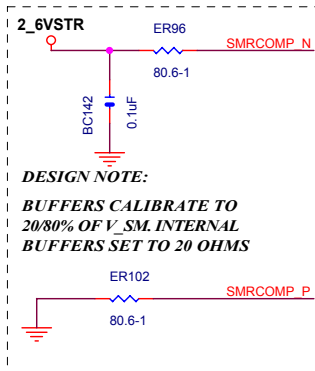
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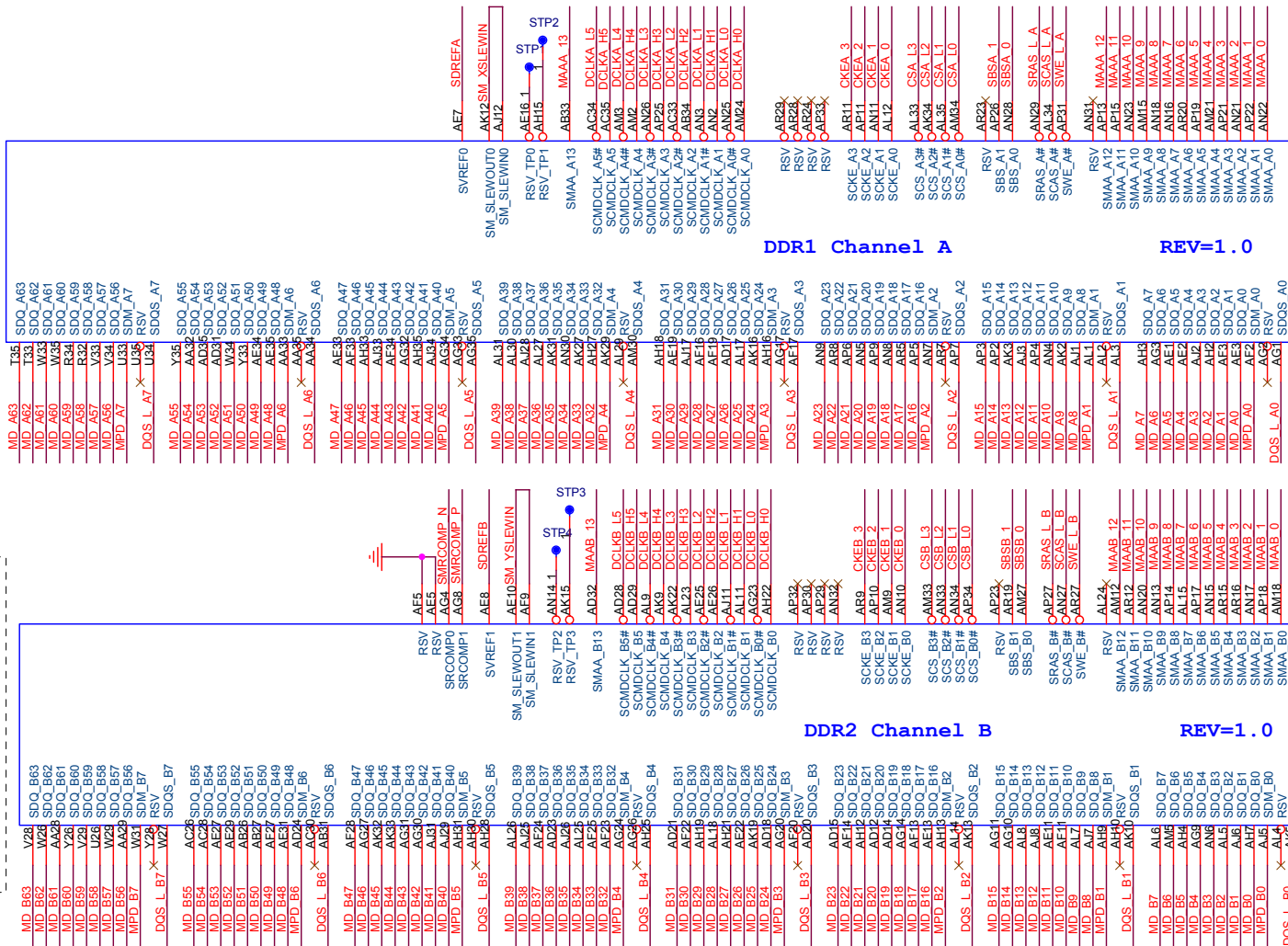








DESIGN NOTE:
BUFFERS CALIBRATE TO
20/80% OF V_{SM} . INTERNAL
BUFFERS SET TO 20 OHMS



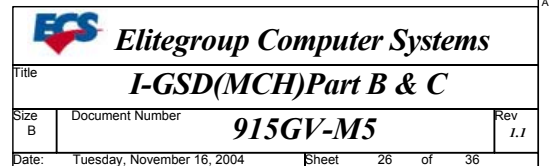
GMCHB
Grantsdale DDR1 MCH_7

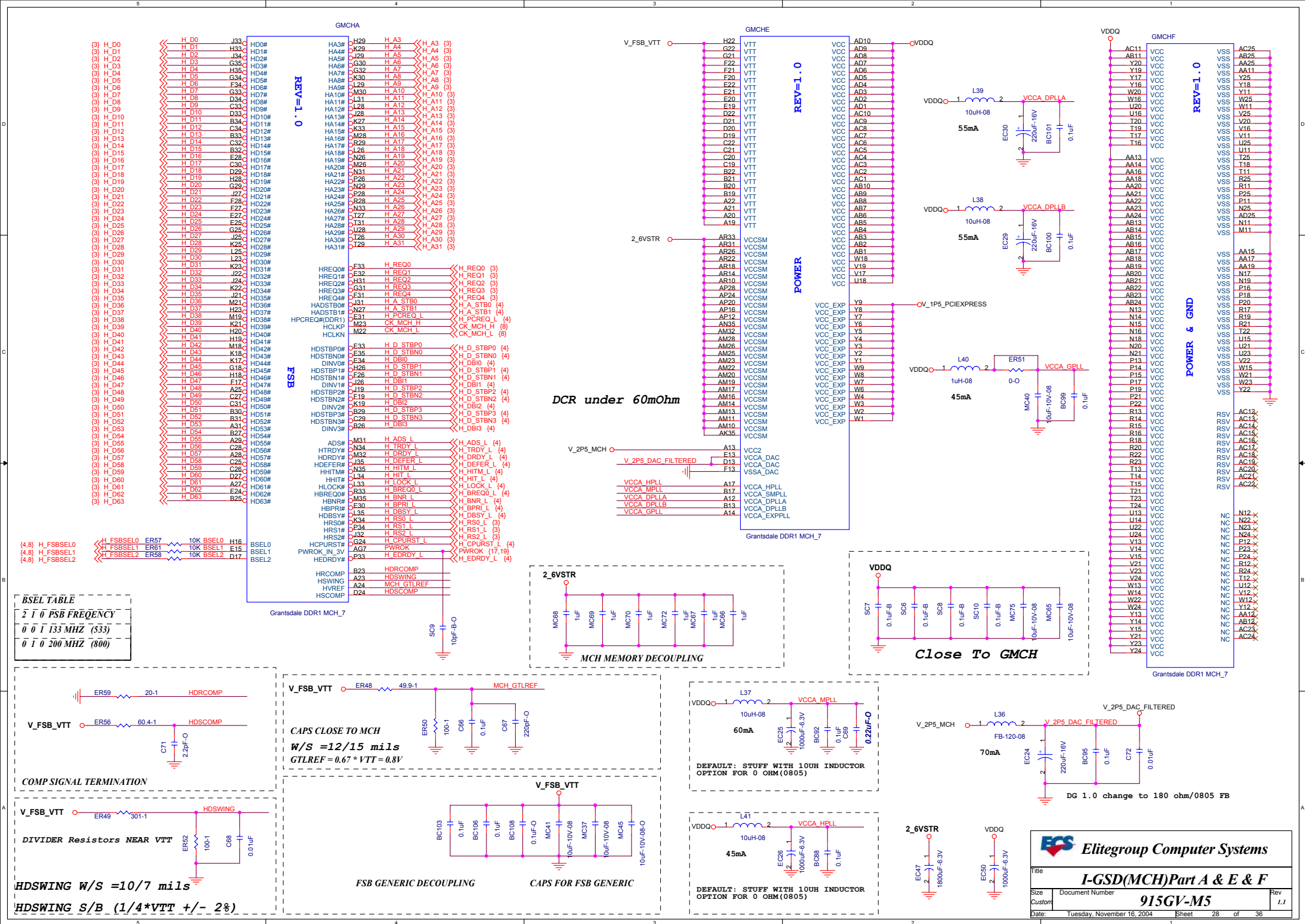
GMCHC
Grantsdale DDR1 MCH_7

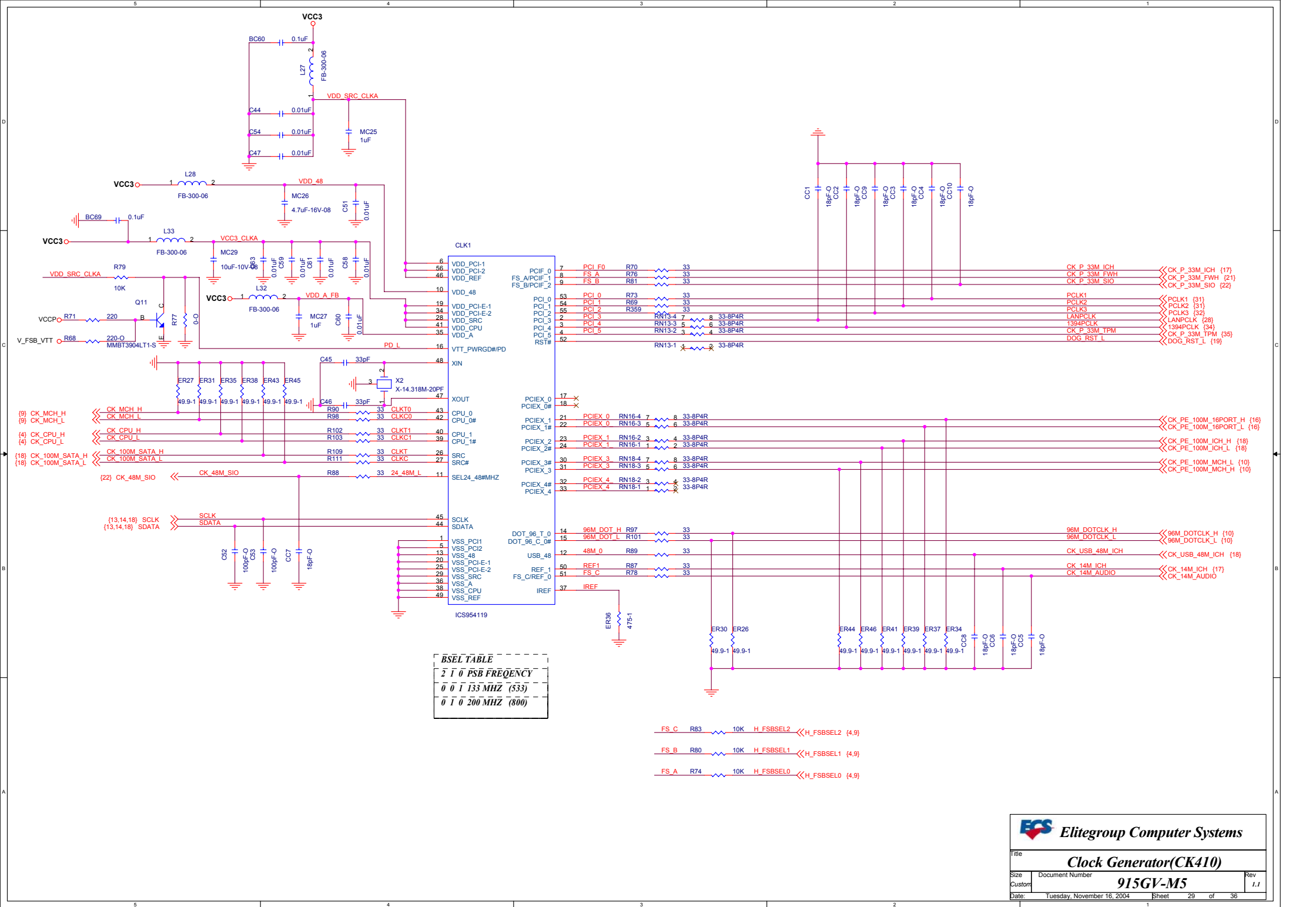
{13} MD_A[0..63]	⋖	MD A[0..63]			
{14} MD_B[0..63]	⋖	MD B[0..63]			
{13} DQS_L_A[0..7]	⋖	DQS_L A[0..7]	{13} CSA_L[0..3]	⋖	CSA L[0..3]
{14} DQS_L_B[0..7]	⋖	DQS_L B[0..7]	{14} CSB_L[0..3]	⋖	CSB L[0..3]
{13} MPD_A[0..7]	⋖	MPD A[0..7]	{13} CKEA[0..3]	⋖	CKEA [0..3]
{14} MPD_B[0..7]	⋖	MPD B[0..7]	{14} CKEB[0..3]	⋖	CKEB [0..3]
{13} MAAA[0..13]	⋖	MAAA [0..13]	{13} DCLKA_L[0..5]	⋖	DCLKA L[0..5]
{14} MAAB[0..13]	⋖	MAAB [0..13]	{13} DCLKA_H[0..5]	⋖	DCLKA H[0..5]

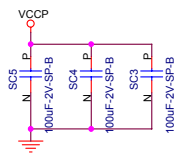
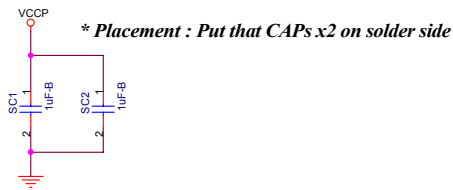
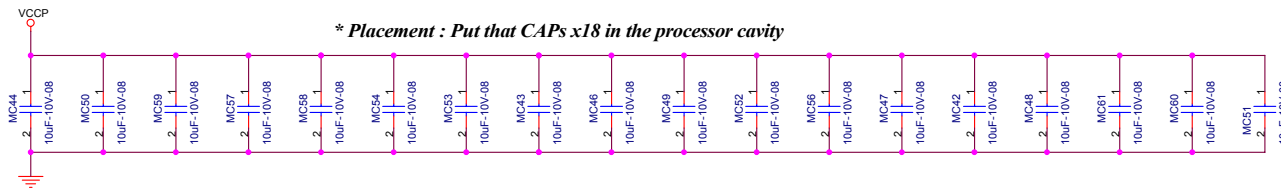
Diagram illustrating the mapping of DCLKB registers to SBSA registers:

- DCLKB_L[0..5]** maps to:
 - SWE_L_A (13)
 - SCAS_L_A (13)
 - SRAS_L_A (13)
 - SWE_L_B (14)
 - SCAS_L_B (14)
 - SRAS_L_B (14)
- DCLKB_H[0..5]** maps to:
 - SBSA_0 (13)
 - SBSA_1 (13)
 - SBSB_0 (14)
 - SBSB_1 (14)
 - SBSB_1 (14)

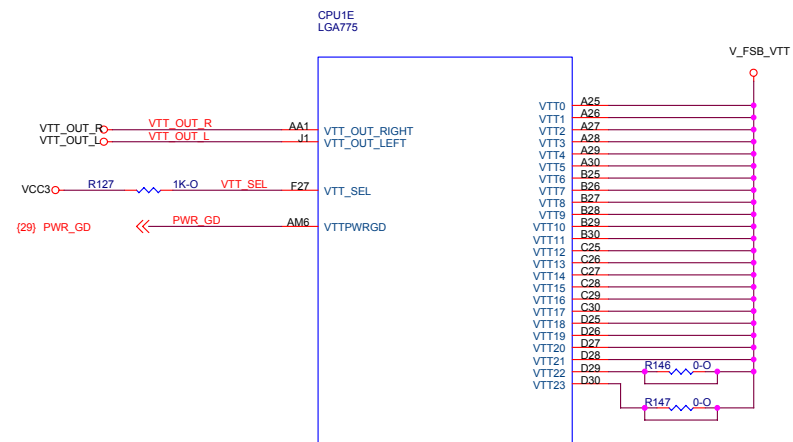








VTT_SEL=0 for the Tejas processor

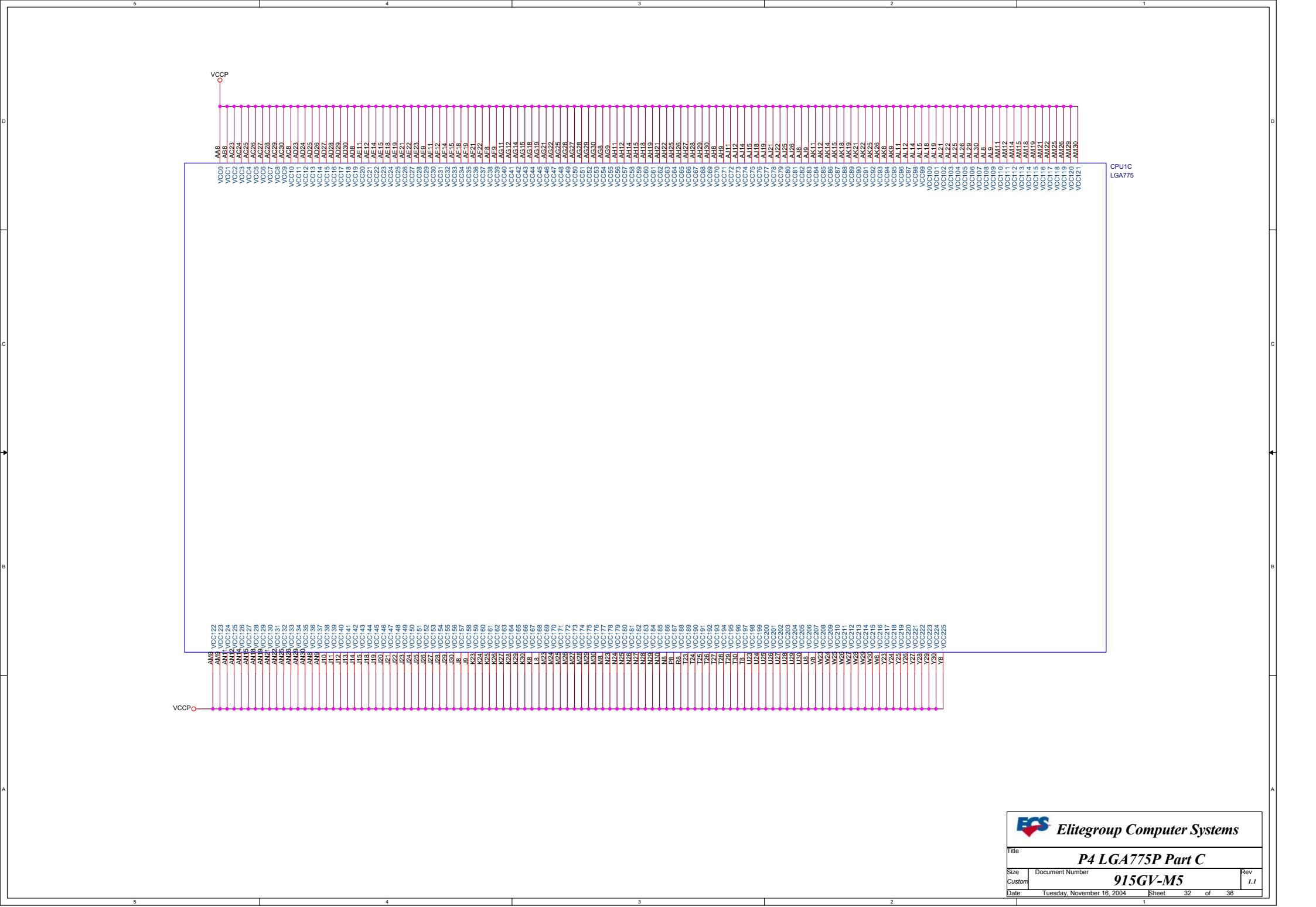


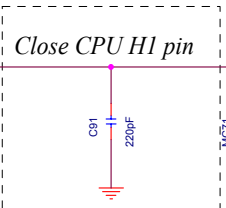
CPU10
LGA775



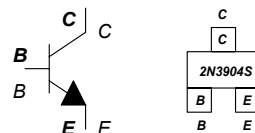
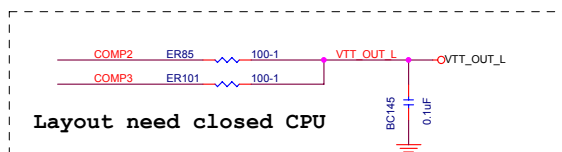
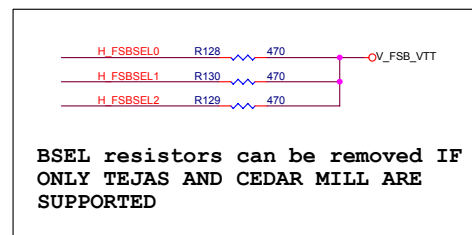
Elitegroup Computer Systems

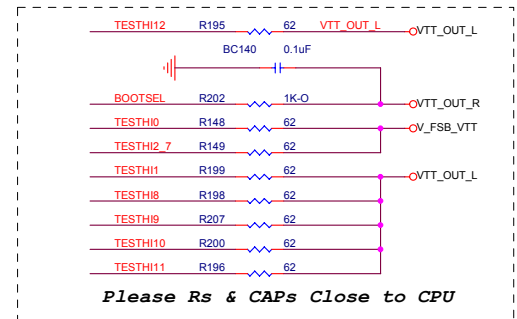
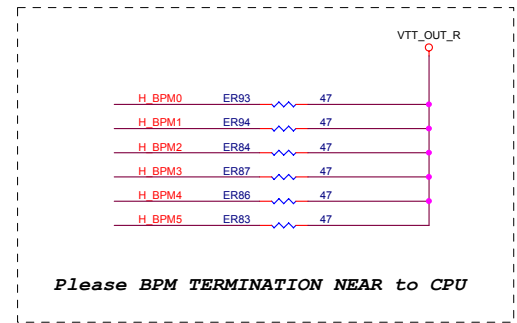
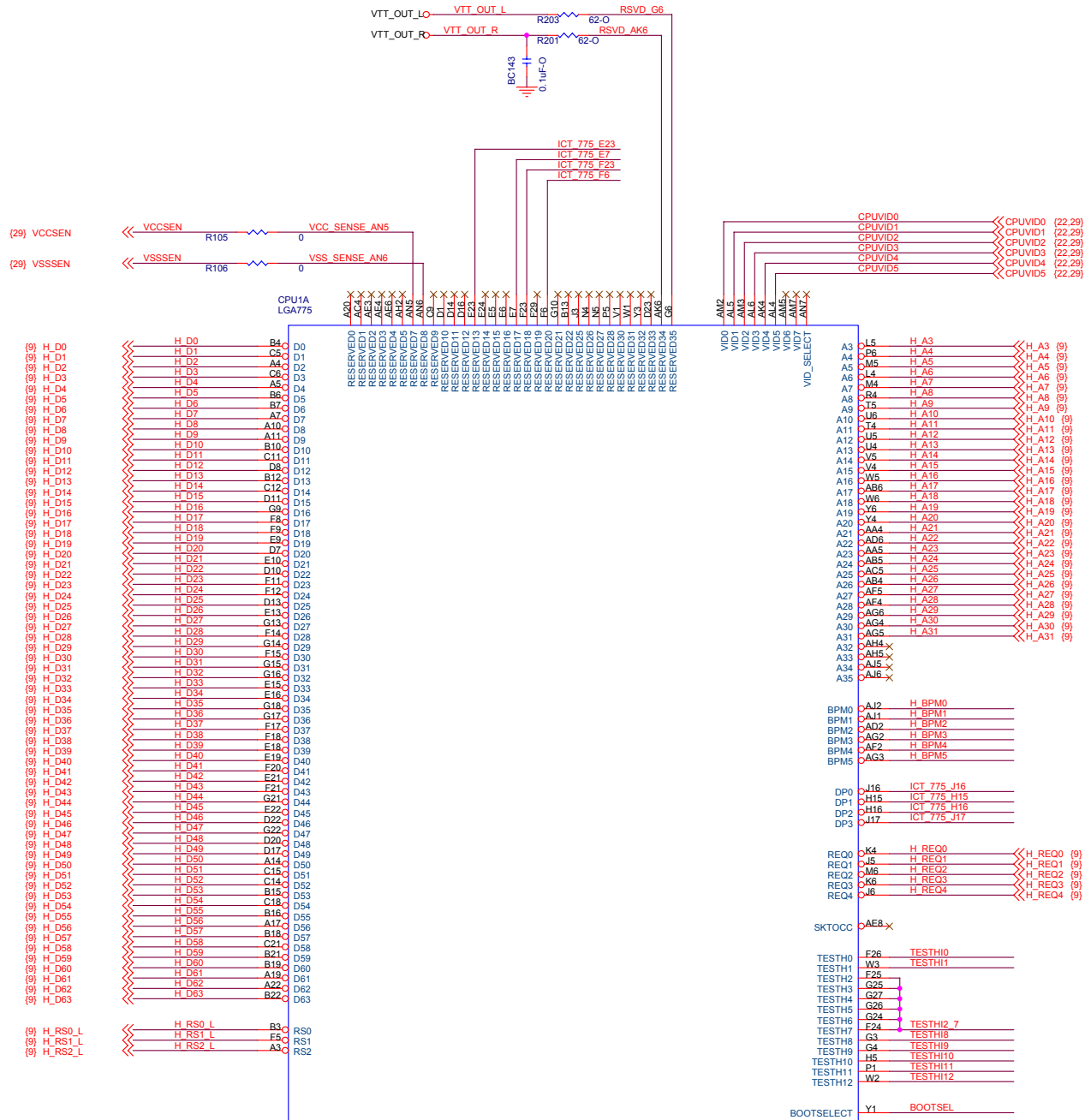
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GTLREF GENERATION CIRCUITS





DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	17	C/D/E/F	PREQ-0	PGNT-0
PCI2	18	D/E/F/G	PREQ-1	PGNT-1
PCI3	19	F/E/H/G	PREQ-2	PGNT-2
1394	20	D	PREQ-3	PGNT-3
LAN	21	E	PREQ-4	PGNT-4

PCB : 244 x 244 mm ; 4 layers

INTEL
P4 Processor
PSC, Tejas -
LGA 775 pin

BW : 4.1GB/s @ FSB : 533MHz & Freq : 133MHz
BW : 6.4GB/s @ FSB : 800MHz & Freq : 200MHz

INTEL
i910GL
1210pin FC-BGA

SIZE : Min 128MB (ONE 256Mb X 16 Single-Sided DEVICES)
SIZE : Max 4GB (Four 512Mb X 8 Double-Sided DEVICES)
BW : 8.5GB/s @ DDR2 :400/533MHz
BW : 6.4GB/s @ DDR : 333/400MHz

DDIMM1: DDR Socket 184P

DDIMM2 : DDR Socket 184P

DDIMM3: DDR Socket 184P

DDIMM4 : DDR Socket 184P

VGA (G only)

Analog Display
RAMDAC: 400MHz
Resolutions Up To 2048x1536@75Hz

BW : 2GB/s (Support Lsoch)

USB1 2 ports
USB2 2 ports
USB3 2 ports
USB4 2 ports
USBLAN 8 ports

USB V2.0

BW : 133MB/s @Freq : 33MHz

INTEL
ICH6
609pin EPGA

PCI1 Slot 120pin @ AD17

PCI2 Slot 120pin @ AD18

PCI3 Slot 120pin @ AD19

Up to Ultra ATA/100
Two IDE Channel

IDE1 40pin

Mic In
Line Out
Line In

Audio Codec
ALC850

AC' 97 & Lan I/F

LPC bus

SATA1 7Pin
SATA2 7pin
SATA3 7Pin
SATA4 7pin

BW : 150MB/s

intel
FWH
32pin PLCC

TPM 1.1

Super I/O
W38627THF
128pin PQFP

VIA 1394

10/100
Lan

USBLAN
RJ45

CONN/
HEADER



Elitegroup Computer Systems

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Rev: D

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